APPLICATION NOTE

- TDA8714 -
8 BIT A/D CONVERTER
DEMOBOARD REFERENCE MANUAL

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- TDA8714 -
8-bit A/D CONVERTER

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Summary

The TDA8714 is a bipolar 8-bit Analog-to-Digital Converter designed for professional applications. It can be used with a sampling frequency up to 75 MHz to convert an analog input signal over a large frequency range with a high signal-to noise ratio (respectively 7.7 and 7.3 effective bits at 4.43 MHz and 10 MHz).
Three versions of the device exist: TDA8714/4, /6 and /7 corresponding to the specification of the sampling rate: 40, 60 or 75 MS/s (see the data sheets in annex of this application note).

Mostly, the applications are located in the professional domain such as video data digitizing, radar pulse analysis, transient signal analysis, medical imaging, and also physics research.

This Application Note describes the design and the realization of the **DEMO 8714** Demoboard using a TDA8714 with an application environment.

Also for the need of demonstration purpose a TDA8712 Digital to Analog Converter is used on the same board to reconstruct the input analog signal after digitizing (see the data sheets in annex of this application note).

CONTENTS

- REFERENCES AND BIBLIOGRAPHY -

[1] - TTL compatible AD/DA converters
Printed Circuit Board - Layout Advice -
Application Note FADC / AN9409 october 1994.

[2] - General-Purpose Linear ICs
PHILIPS Data Handbook IC11 1995.

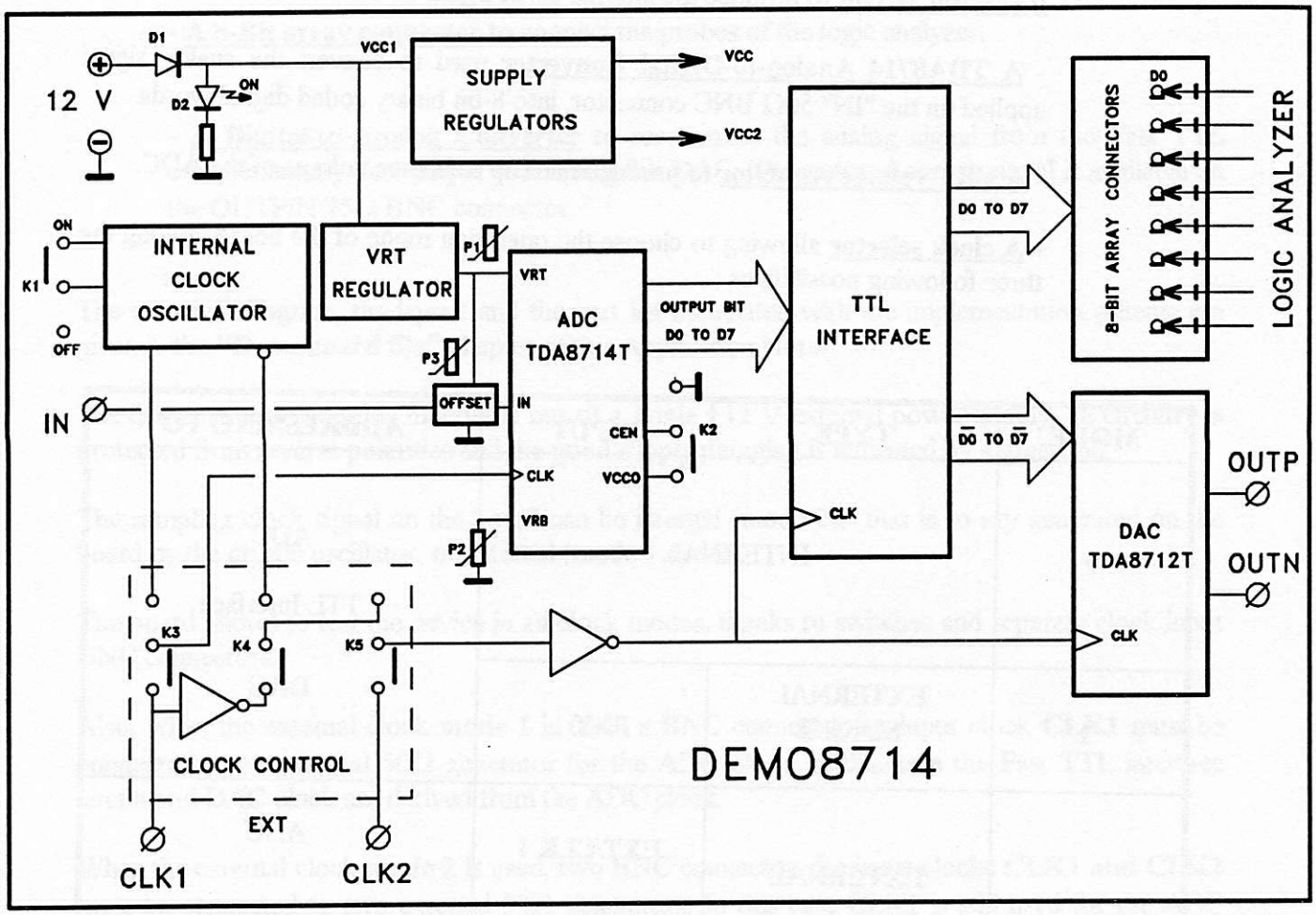
[3] - ECLinPS MOTOROLA Device Data DL140 Q1/89.

[4] - Surface Mounted Semiconductors
PHILIPS Data Handbook SC10b 1994.

[5] - FAST TTL Logic Series
PHILIPS Data Handbook IC15 1992.

1. PRINCIPLE AND DESCRIPTION

The principle of the Demoboard, which is described in this Application Note, is shown on the **Figure 1**.



- FIGURE 1 -

The different blocks constituting the board are the following :

- **A power supply regulator circuit** used to supply all the circuitry on the board.

- **An ECL internal Quartz Oscillator** which drives an associated **ECL to TTL translator circuit** to produce the internal clock signal on the board.

- **A TDA8714 Analog-to-Digital Converter** used to convert the analog signal applied on the "IN" 50Ω BNC connector, into 8-bit binary coded digital words.

- **A VRT voltage regulator** to produce the Top reference voltage of the ADC.

- **A clock selector** allowing to choose the operation mode of the board, among the three following possibilities :

<table>
<tr><th>MODE</th><th>TYPE</th><th>INPUT</th><th>ADDRESSING TO</th></tr>
<tr><td>0</td><td colspan="2">INTERNAL</td><td rowspan="2">ADC
TTL Interface
DAC</td></tr>
<tr><td>1</td><td>EXTERNAL
SINGLE</td><td>EXT 1</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">EXTERNAL
DOUBLE</td><td rowspan="2">EXT/CLK 1

EXT/CLK 2</td><td>ADC</td></tr>
<tr><td>TTL Interface
DAC</td></tr>
</table>

A Fast TTL Interface decision circuit used to recover theADC data output synchronized on the clock sampling edge rising. The recovered data are directly addressed on a special probe connector available on the board, to evaluate the TDA8714 in the application in the digital domain.

- **A 8-Bit array connector** to connect the probes of the logic analyzer.

- **A Digital-to-Analog Converter** to reconstruct the analog signal from the Fast TTL complementary data output addressing this DAC. The restored analog signal is available on the OUTP/N 75Ω BNC connector.

The electrical diagram, the layout and the part list associated with the implementation scheme are given in the **"Demoboard file"** chapter of this Application Note.

The demonstration board is functional out of a single +12 V external power supply, all circuitry is protected from reverse polarities and the good supply plugging is indicated by a green led.

The sampling clock signal on the board can be internal (mode 0), that is to say generated on the board by the crystal oscillator, or external (mode 1 and 2).

The board allows to test the device in all clock modes, thanks to switches and separate clock input BNC connectors.

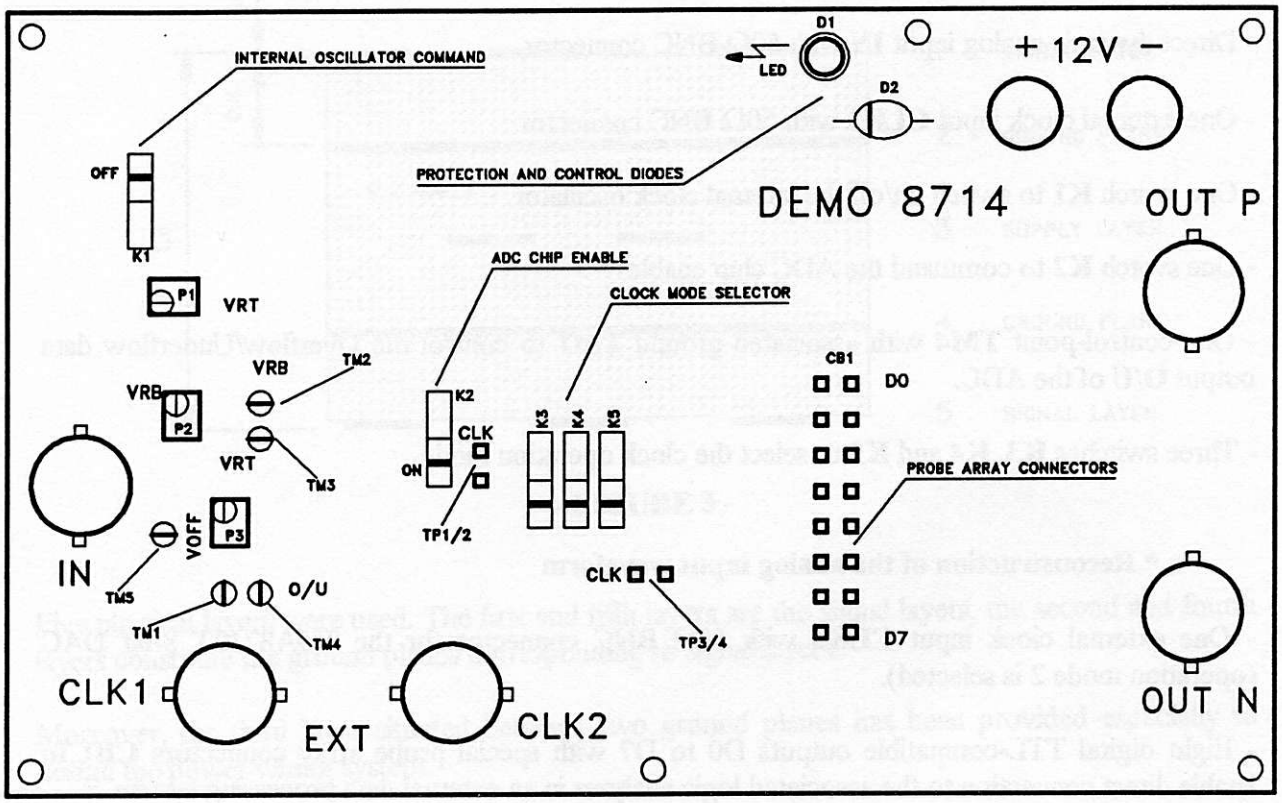
Also, when the external clock **mode 1** is used, a BNC connector for input clock **CLK1** must be connected to an external 50Ω generator for the ADC clock, in this case the Fast TTL interface circuit and DAC clock are derived from the ADC clock.

When the external clock **mode 2** is used, two BNC connectors for input clocks **CLK1 and CLK2** must be connected to two external 50Ω generators. In this case CLK1 is still used for the ADC clock, but CLK2 is used for the Fast TTL interface circuit and DAC clock.

Before using the board, please choose your mode and refer to the corresponding "clock operating mode" chapter, to verify that the switches are correctly set.

2. OVERALL VIEW OF THE BOARD

The whole implantation of this Demoboard is shown in **Figure 2**.



- FIGURE 2 -

The different available connection plugs, trimmers, switches and test-points on the board are, for :

*** DC voltage values adjustment values**

. Three chip trimmer potentiometers **P1**, **P2**, **P3** and three control-points **TM3**, **TM2**, **TM5** to adjust respectively the VRTop and VRBottom Reference Voltages and the VOFF analog input offset of the ADC.

*** Evaluation of the TDA8714**

- Direct dynamic analog input **IN** with 50Ω BNC connector.

- One external clock input **CLK1** with 50Ω BNC connector.

- One switch **K1** to switch on/off the internal clock oscillator.

- One switch **K2** to command the ADC chip enable.

- One control-point **TM4** with associated ground **TM1** to control the Overflow/Underflow data output **O/U** of the ADC.

- Three switches **K3**, **K4** and **K5** to select the clock operation mode.

*** Reconstruction of the analog input waveform**

- One external clock input **CLK2** with 50Ω BNC connector for the TDA8712T 8-bit DAC (operation mode 2 is selected).

- Eight digital TTL-compatible outputs D0 to D7 with special probe array connectors **CB1** to enable direct connection to the associated logic analyzer in an external data processing system.

- Two special probe test-points **TP1/2** and **TP3/4** to control the ADC clock, the Fast TTL interface circuit and the DAC clock.

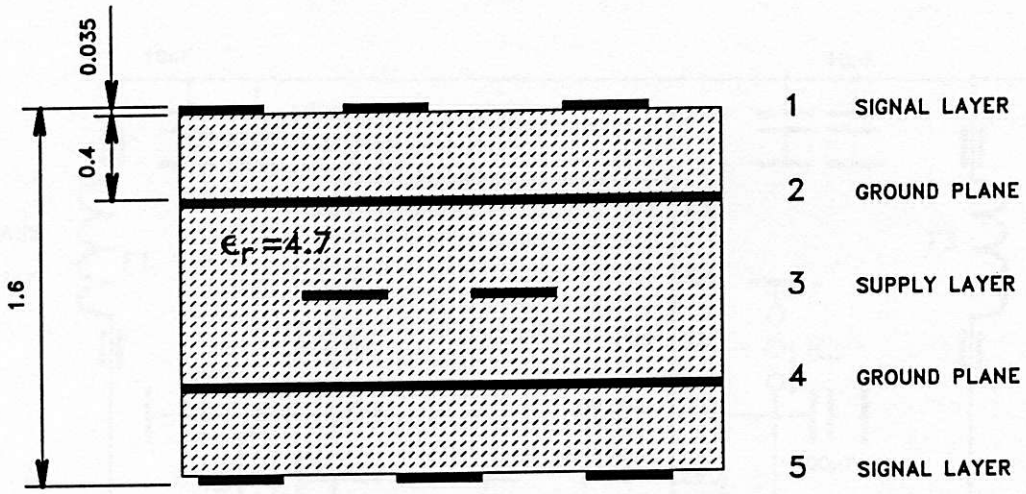
- Two differential analog outputs **OUTP/N** with 75Ω BNC connectors.

*** General power supply**

- Two female banana connectors **+12V** and **-** (GND) with a standard spacing to connect to a banana/BNC adaptor.

3. TECHNOLOGICAL CONCEPT

The practical design has been made on a multilayer Printed Circuit Board of european size. The technological concept used to make this multilayer PCB is given in the Figure 3.



- FIGURE 3 -

Five physical layers were used. The first and fifth layers are the signal layers, the second and fourth layers constitute the ground planes corresponding to signal layers.

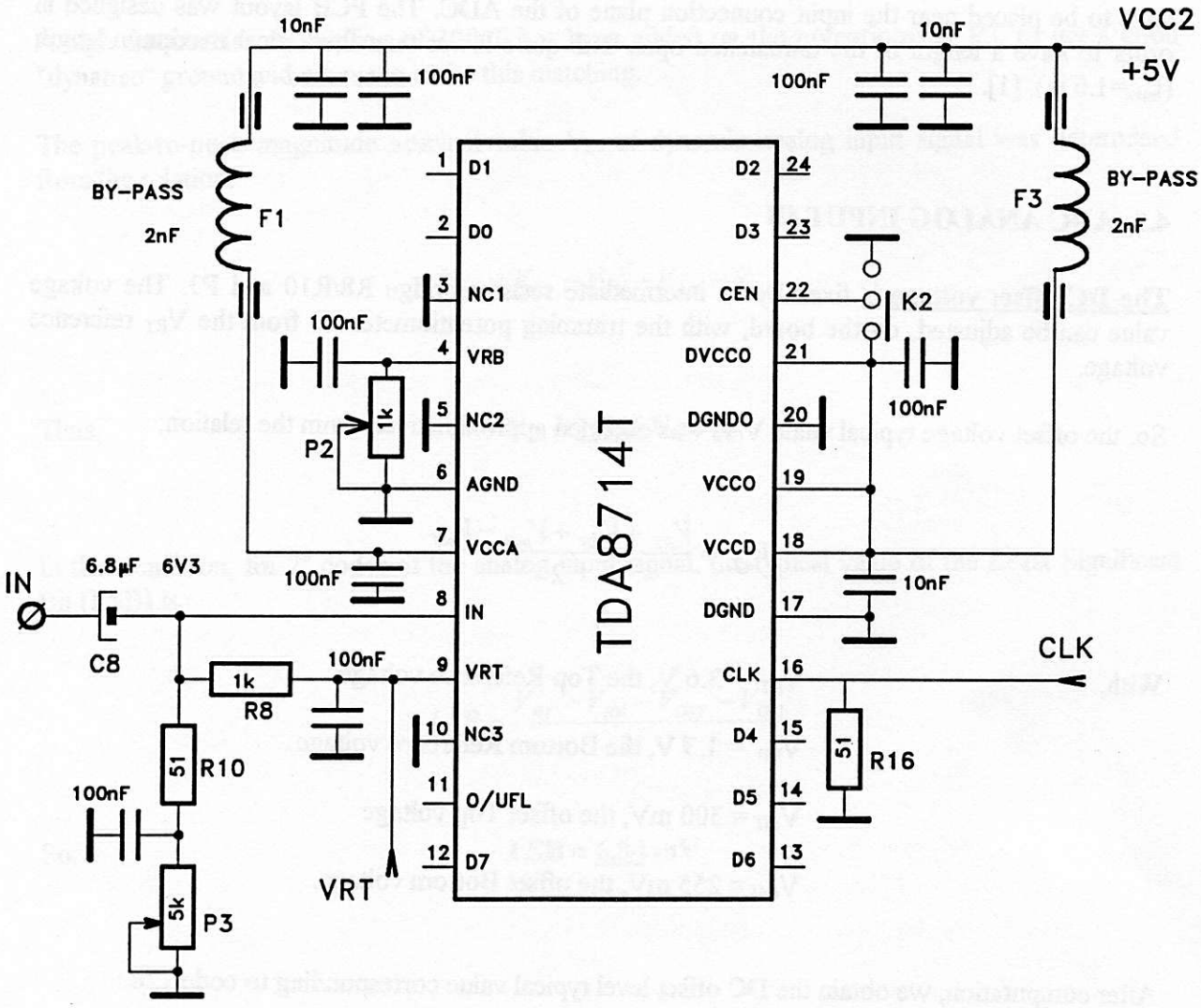
Moreover, the third layer situated between two ground planes has been provided especially to design the power wiring system.

The dielectric substrate used is an Epoxy Glass resin having a relative permittivity of 4.7 and a copper thickness of 35 µm. The metallized via hole technic was employed to make all necessary interconnections between layers.

The global thickness of PCB is about 64 mils (1.6 mm) with a thickness between layer of 16 mils (0.4 mm). So, all the matched lines were designed with the microstrip technology, [1].

4. SPECIAL FEATURES OF THE TDA8714

In order to obtain the optimal performances, the advised Application scheme of the TDA8714 is given on the **Figure 4**.



- FIGURE 4 -

4.1 ADC INPUT MATCHED LINES

The Analog and Clock lines addressing the ADC are dynamically matched to 50Ω on the board. The microstrip technology was used to make the matched lines. Thereby, the width of these matched lines has been computed from the Kaup's formulas.

To minimize the under/overshoots levels on the ADC clock input signal, the 50Ω terminated loads have to be placed near the input connection plane of the ADC. The PCB layout was designed in order to have a length of the unmatched open stub quite lower than theoretical maximum length (l_{max}=1.6 in), [1].

4.2 ADC ANALOG INPUT IN

The DC offset voltage is fixed by an intermediate resistor bridge R8/R10 and P3. The voltage value can be adjusted, on the board, with the trimming potentiometer P3 from the V_{RT} reference voltage.

So, the offset voltage typical value V_{OFF} was obtained approximatively from the relation:

$$V_{off} = \frac{V_{RT} + V_{RB} + V_{osB} - V_{osT}}{2}$$

With,

V_{RT} = 3.6 V, the Top Reference voltage

V_{RB} = 1.3 V, the Bottom Reference voltage

V_{osT} = 300 mV, the offset Top voltage

V_{osB} = 255 mV, the offset Bottom voltage.

After computation, we obtain the DC offset level typical value corresponding to code 128 :

$$V_{OFF} \approx \underline{2.428}\ V$$

Moreover, to insure a sufficient analog input stability, the offset bridge resistor current I_{POFF} was fixed at 1.2mA taking into account the specified high level analog input current I_{IH} (180 µA) of the ADC.

The dynamic analog input is connected through a 6.8 µF AC coupling to the external generator via a 50Ω microstrip matched line and a BNC plug-in connector.

A high frequencies decoupling of 100nF has been added on the potentiometer P3, to get a good "dynamic" ground and allows to make this matching.

The peak-to-peak magnitude nominal value V_{IN} of dynamic analog input signal was determined from the relation:

$$V_{IN} = V_{RT} - V_{RB} - V_{osT} - V_{osB}$$

Thus, $\mathbf{V_{IN} \approx \underline{1.745}\ V\ p.\text{-}p}$

In this condition, for 2^8 codes of the analog input signal, the typical value of the Least Significant Bit (LSB) is :

$$LSB = \frac{V_{RT} - V_{RB} - V_{OST} - V_{OSB}}{2^8 - 1}$$

So, $\mathbf{LSB \approx \underline{6.84}\ mV}$.

4.3 DATA OUTPUT DO TO D7

Taking into account the output equivalent DC impedance of the TDA8714 of about 90Ω and the copperplate precision of the PCB layout, all the data output lines are directly addressed to a TTL interface circuit with 75Ω microstrip lines.

The lengths l_D of these lines were determined taking into account the following values, [1] :

- The specified maximum output capacitance load C_L = 15 pF.
- The maximum input capacitance of TTL interface C_{IN} = 5 pF.
- The distributed capacitance on the line C_0 = 0.76 pF/cm.

In order to satisfy :

$$I_D \leq \frac{C_L - C_{IN}}{C_o}$$

4.4 ADC ANALOG AND DIGITAL POWER SUPPLIES

One power line VCC2 only is used to supply the ADC under +5 Volts delivered on the output of the IC regulator type MC7805CT of the general power supply circuit.

Consequently, to improve the dynamic rejection of the clock signal on the supply line two SMD bypass pi type filters were implanted on the board near the ADC to separate each power pin of the device.

Moreover, the PCB layout has been designed so that the power supply line end arrives close to the VCCD side. This point is perfectly decoupled with 100nF in parallel 10nF ceramic capacitors.

4.5 REFERENCE VOLTAGES VRT AND VRB

The Top Reference voltage V_{RT} of 3.6 Volts is obtained from a specific IC precision voltage regulator implanted on the board. The output voltage of the regulator is directly applied on the Top pin of the ADC, a 100 nF ceramic capacitor placed close to this point constitutes an effective decoupling.

For the electrical diagram and description of the proposed circuit please see "VRT voltage regulator" paragraph enclosed in the following chapter.

The Bottom Reference voltage V_{RB} of 1.3 Volt is obtained by the shift voltage across the trimmer potentiometer P2 = R_{BOT}, from the reference current I_{REF} in the ADC resistor ladder.

Taking into account :

- The typical values of the quantization ladder parameters at 25°C :

$R_{LAD} = 200\ \Omega$	$TC°_{RLAD} = 1200$ ppm/°K	$I_{REF} = 11.5$ mA
$V_{RT} = 3.6$ V	$V_{osT} = 300$ mV	
$V_{RB} = 1.3$ V	$V_{osB} = 255$ mV	

- The thermal coefficient of the output voltage of the VRT regulator :

$$TC°_{VRT} = 150 \text{ ppm/°K}$$

- The thermal coefficient of the external Bottom resistor R_{BOT} obtained with the adjustment of trimmer potentiometer P2 :

$$TC°_{RBOT} = 100 \text{ ppm/°K}.$$

It is possible to evaluate the variation of all the relevant parameters of the quantization ladder due to the working thermal ambient conditions (T_{amb} between 0°C up to 70°C), from the general relation :

$$A(T_{amb}) = A_{nom}|_{25°C}\left[1 + TC°\left(T_{amb} - 25°\right)\right]$$

where, A and TC° are the respectively considered nominal parameter and thermal coefficient values. The results obtained after computation are the following :

T_{amb}	0°C	25°C	70°C
V_{RT}	3.587 V	3.600 V	3.624 V
V_{RB}	1.319	1.300	1.271
V_{osT}	0.296	0.300	0.308
V_{osB}	0.252	0.255	0.262
R_{LAD}	194.0 Ω	200.0 Ω	210.8 Ω
R_{BOT}	112.7	113.0	113.5
R_{osB}	21.5	22.2	23.4
R_{osT}	25.3	26.1	27.5
I_{REF}	11.7 mA	11.5 mA	11.2 mA

Consequently, the method employed to produce the reference voltages, allows to obtain a low voltage drift for LSB and V_{128} code level values, from 0°C up to 70°C, that is to say :

$\Delta LSB \approx -90.0\ \mu V$ at $T_{amb} = 0°C$

$\Delta LSB \approx 150.0\ \mu V$ at $T_{amb} = 70°C$

$\Delta V_{128} \approx \pm 3.0\ mV$ $0°C < T_{amb} < 70°C.$

Taking into account the operating ambient temperature of the demoboard, the maximum values and the voltage drift of the analog signal magnitude V_{IN} which can be applied on the demoboard are the following :

T_{amb}	0°C	70°C
V_{IN}	1.720 V p.-p	1.783 V p.-p
drift / 25°C	- 25 mV	38 mV

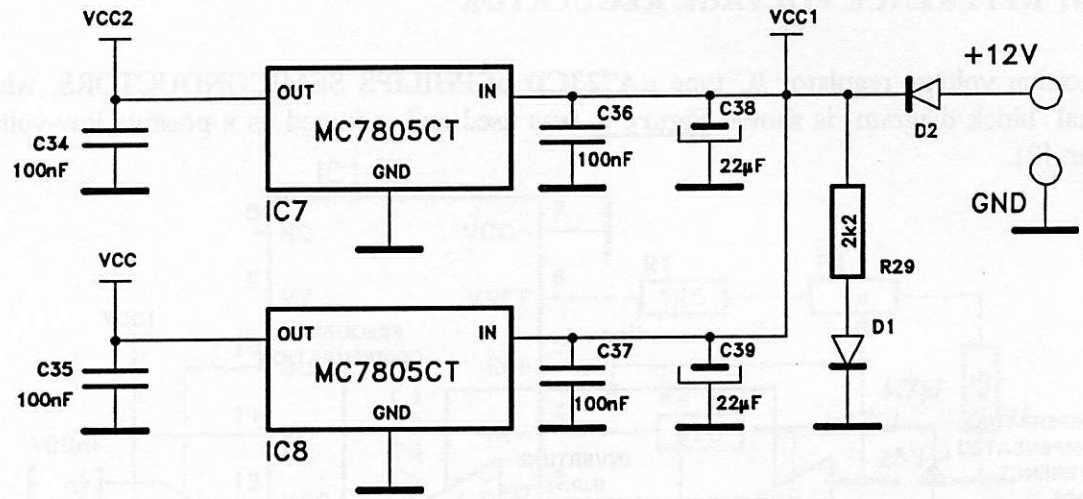
Moreover, taking into account the thermal coefficients of the offset bridge resistor of 200 ppm/°K for R8,R18 and 100 ppm/°K for P3, the maximum of voltage drift values of the offset level and the typical variations Δ between V_{128} and V_{OFF} are :

T_{amb}	0°C	70°C
ΔV_{OFF}	- 7 mV	+ 13 mV
$\Delta(V_{128} - V_{OFF})$	- 4 mV	+ 10 mV

5. ENVIRONMENT CIRCUITS

5.1 GENERAL POWER SUPPLY

The proposed electrical diagram is shown on the **Figure 5**. This circuit uses two MC7805CT IC voltage regulator IC7 and IC8 directly mounted on the board and supplied from an external power unit of 12V/0.5A, the operation of this circuit is possible from an external voltage comprised between 10 Volts and 15 Volts.



- FIGURE 5 -

This circuit does the regulation and stabilization of the supply voltage of all the circuitry from the VCC1 voltage value obtained after the protection diode D2. Two stabilized voltages VCC and VCC2 of + 5 Volts are available on the demoboard with the following distribution :

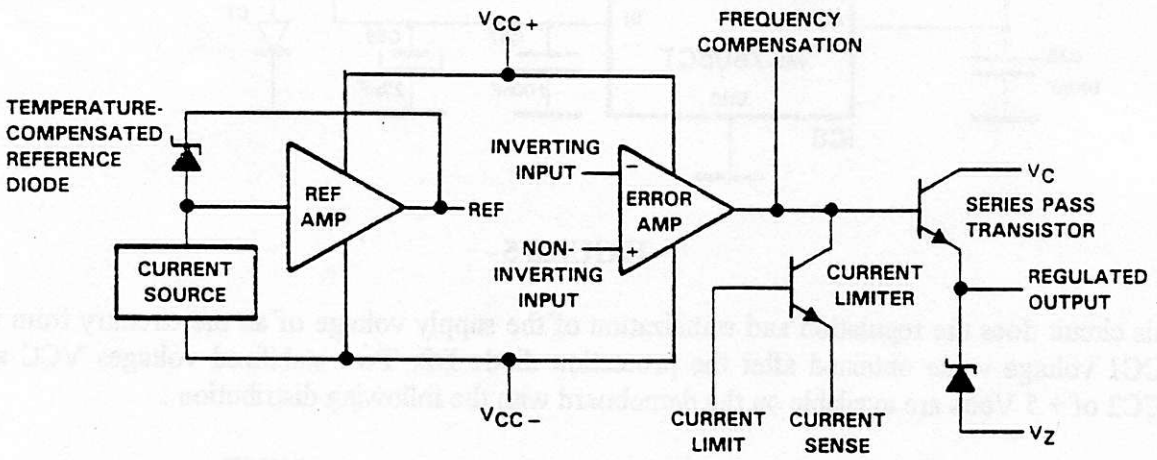
VCC	VCC2
Fast TTL circuitry	Xtal oscillator
D/A Converter TDA8712T	ECL to TTL translator
	A/D Converter TDA8714T

The type BYV27 Silicium diode D2 ensures the protection of all the circuitry from reverse polarities, the good supply plugging is indicated by a green led diode D1, too.

Under the external power supply nominal value + 12 Volts, the consumptions on VCC and VCC2 are respectively 95 mA and 194 mA. Consequently with this same condition, the dissipated power on IC7 is about 1.2 W and on IC8 about 600 mW.

5.2 TOP REFERENCE VOLTAGE REGULATOR

The precision voltage regulator IC type **µA723CD** of PHILIPS SEMICONDUCTORS, whose functional block diagram is shown **Figure 6**, was used and mounted as a positive low-voltage regulator, [2].

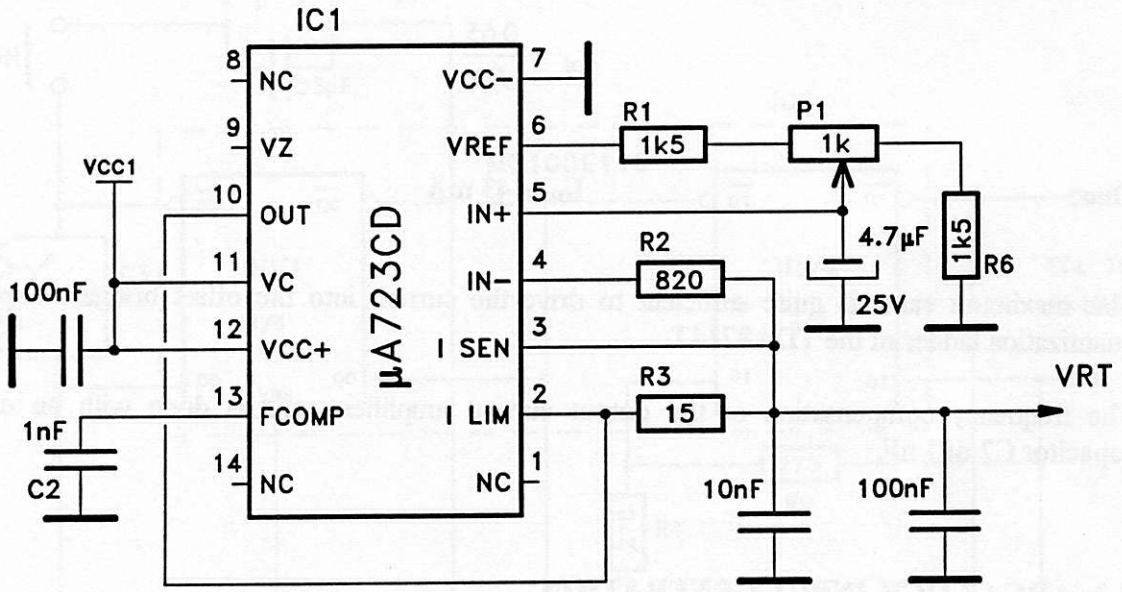


- FIGURE 6 -

The proposed circuit is shown in the **Figure 7**.

The voltage level VCC1 obtained on the cathode of the protection diode D2, is applied on the VCC+ (pin 12) of the device.

The nominal reference level of 3.6V is obtained from the voltage level supplied on the VREF (pin 6) of the µA723CD. A bridge resistor R1/R6 with trimmer potentiometer P1 allows to adjust the reference level value on the no-inverting input IN+ (pin 5) of the IC. Thereby, the dynamic balance of the integrated error amplifier is made with R2 connected between the inverting input IN- (pin 4) and the V_{RT} output voltage point.



- FIGURE 7 -

Moreover, to obtain a good output stability, the value of R2 must be equivalent to the reference bridge resistor dynamic value.

Consequently taking into account R1, R6 and P1 values we have chosen a resistor value **R = 820 Ω**.

The output limiting current is ensured from the start conduction of the internal IC limiter current transistor that is to say when the VBE voltage level it is about 0.65 V.

So, the resistor R3 connected between I_LIM (pin 2) of the IC and the regulated point V_{RT} output, allows to control the output limiting current I_{OL}. With, R3=15Ω the limiting current value I_{OL} is obtained from the relation :

$$I_{OL} = \frac{0.65}{R3}$$

Thus, **I_{OL} = 43 mA**

This maximum value is quite sufficient to drive the current into the offset bridge resistor and quantization ladder of the TDA8714T.

The frequency compensation of the output current amplifier stage is done with an external capacitor C2 of 1 nF.

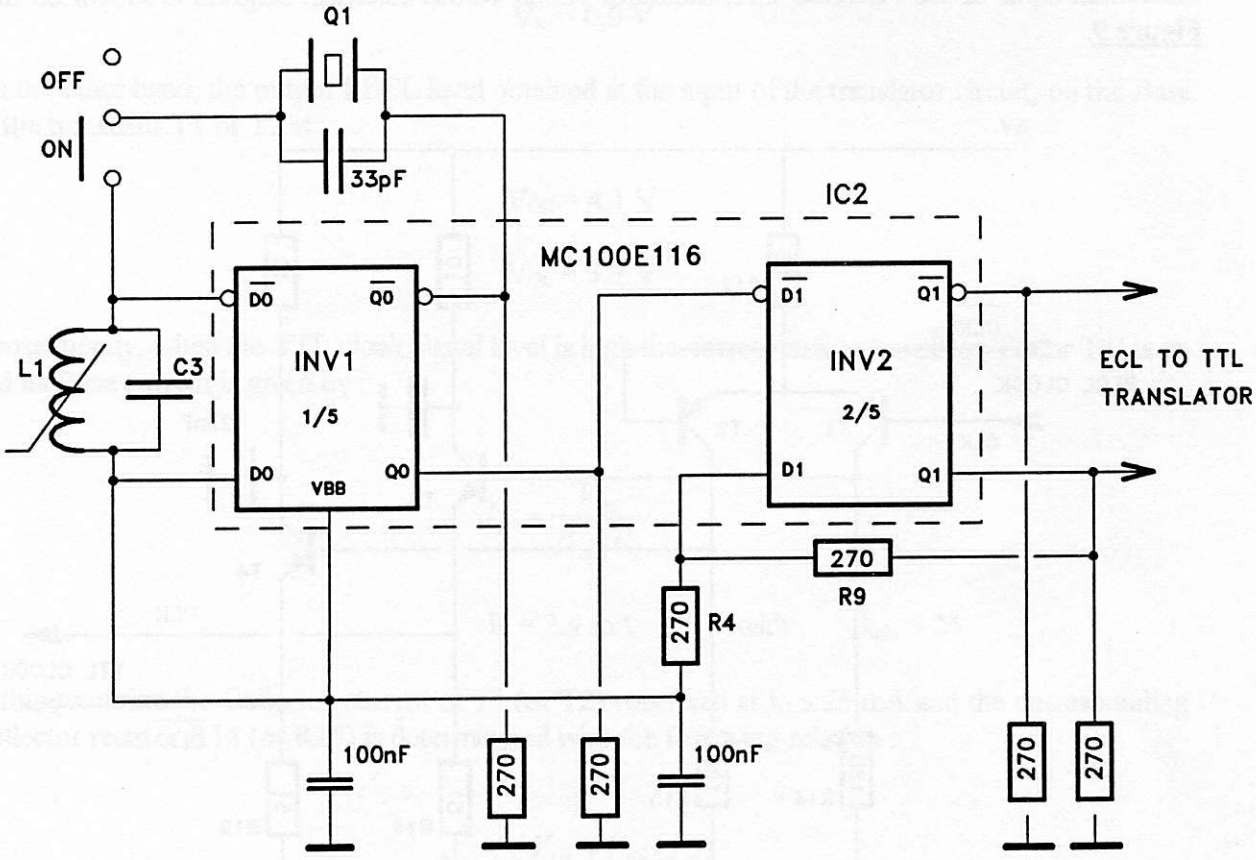
5.3 ADC CLOCK INPUT GENERATION

On the Demoboard a specific circuit has been designed to produce the clock signals addressing to ADC and TTL interface circuit. Motorola IC "ECL in PS" family [3], was used to design a PECL mounting crystal oscillator of which the electrical diagram is shown on the **Figure 8**.

So, one quint differential line receiver IC type MC100E116 of the 100E series, in 28-pin PLCC package was soldered directly on the board. Two line receivers INV1 and INV2 contained in the IC were used to make the functions of oscillating and shaping.

The first ECL gate INV1 is associated in positive feedback with the overtone Xtal Q1. The antiresonance harmonic frequency is selected from the tuned inductance L1 of the tank circuit L1 C3.

This tuned inductance has been made with 4 turns of enameled copper conductor of 0.30 mm of diameter, and mounted on the type 7.1S HF coil assemblies from TOKO.

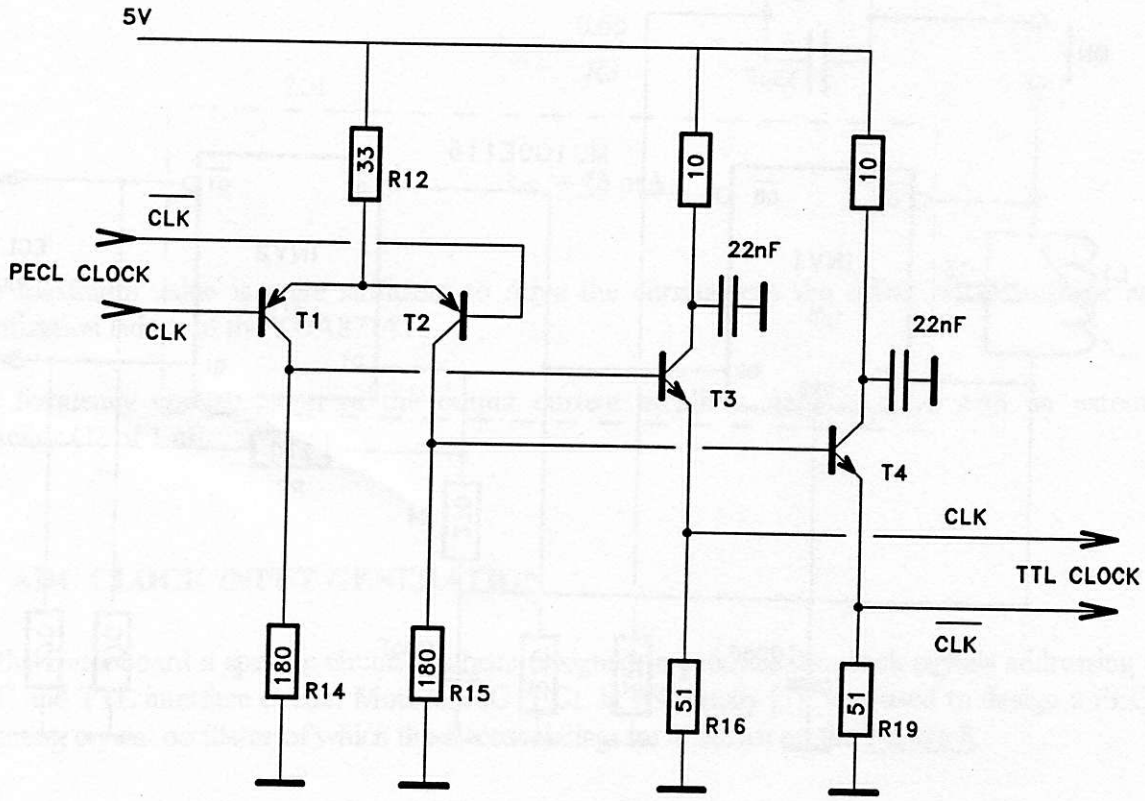


- FIGURE 8 -

Depending on the ADC type (TDA8714T/4 /6 or /7) implanted on the demoboard, the values of the Xtal Q1 and capacitor C3 are the following :

ADC type	Q1	C3
TDA8714T/4	40.00 MHz	120 pF
TDA8714T/6	60.00 MHz	56 pF
TDA8714T/7	75.00 MHz	15 pF

The first ECL gate output drives the input of the Schmit trigger circuit constituted of the second ECL gate INV2 and of the associated resistors R4 and R9. This second ECL gate output drives the differential input of the PECL to TTL translator circuit whose electrical diagram is shown on the **Figure 9**.



- FIGURE 9 -

This PECL to TTL translator circuit was made with discret SMD components. It is made of :

- a differential stage constituted of the PNP transistors T1 and T2 type BFT92,
- the two associated output following stages constituted of the NPN transistors T3 and T4 type BFR106, [4].

The outputs translator stage T3 and T4 are loaded with $R_L = 50\Omega$ and able to supply a TTL clock signal whose high and low levels are the following :

$$V_{IH} = 3.0\ V$$

$$V_{IL} = 0.0\ V$$

On the other hand, the output PECL level obtained at the input of the translator circuit, on the Base of the transistor T1 or T2 is :

$$V_{OH} = 4.1\ V$$

$$V_{OL} = 3.3\ V$$

Consequently, when the TTL clock signal level is high the corresponding transistor T3 (or T4) is on and its Base current is given by :

$$I_B = \frac{V_{IH}}{\beta_{min} R_L}$$

$I_B = 2.4\ mA$ with $\beta_{min} = 25$

In this condition the Collector current of T1 (or T2) was fixed at $I_C \leq 25\ mA$ and the corresponding Collector resistor R14 (or R15) is determinated with the following relation :

$$R14 = \frac{V_{IH} + V_{BE}(T3)}{I_c(T1) - I_B(T3)}$$

$$R14 = R15 = 180\Omega$$

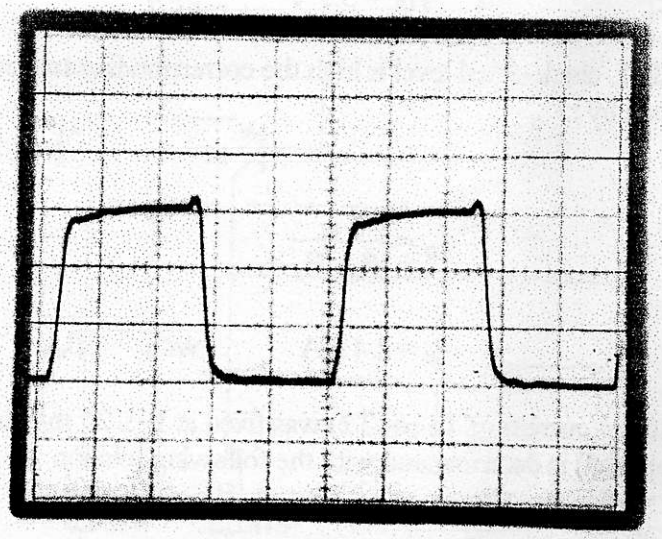
Thereby, the Emitter resistor R12 of T1 and T2 can be evaluated according to :

$$R12 = \frac{VCC2 - (V_{CL} + V_{BE})}{I_e(1+1/\beta_{min})}$$

Thus R12 = 33 Ω with β_{min} (T1) = 20

The waveform of the internal clock signal obtained on a 40MS/s demoboard is shown by the diagram of the **Figure 10**, with the following performances :

High level	V_{clkH} = 3.0 V	Rise/Fall time	$t_{r/f}$ = 1.5 ns
Low level	V_{clkL} = 0.0 V	Duty cycle	η = 50 %

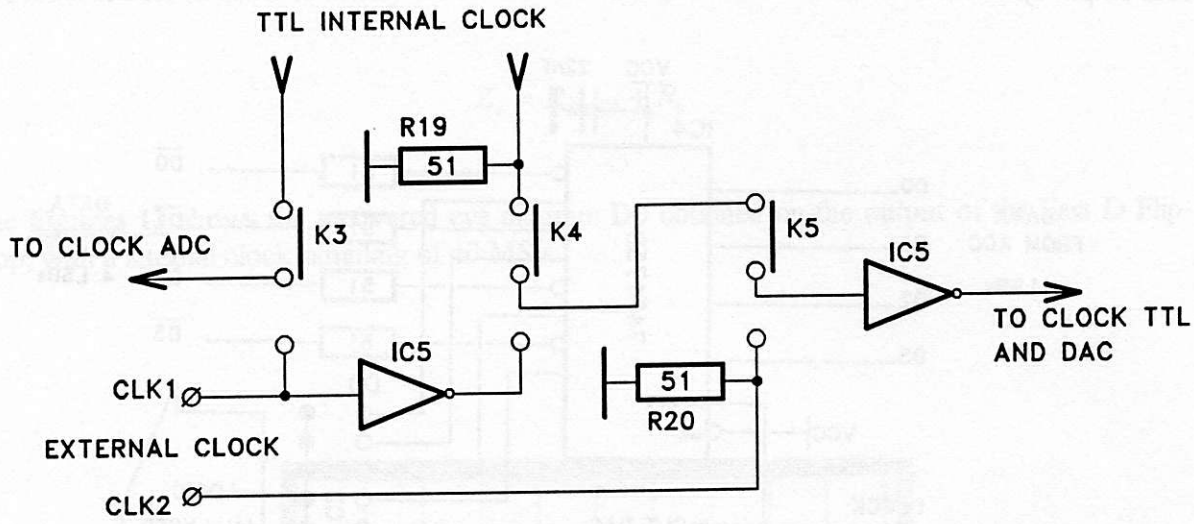


↑ 1 V/div → 5 ns/div

- FIGURE 10 -

5.4 CLOCK SELECTOR CIRCUIT

The electrical diagram of the proposed circuit is shown on the **Figure 11**. It uses three switches 1C/2P and two inverters type **74F04D** of the Fast TTL family, [5].



- FIGURE 11 -

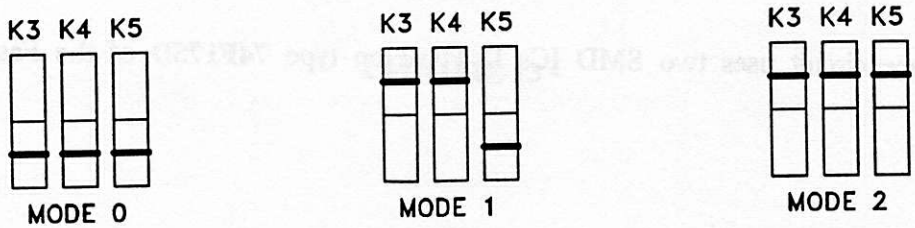
This circuit allows to select the operating clock mode of the demoboard among three possibilities.

Mode 0 : The Internal clock mode.

Mode 1 : The External single clock mode CLK1.

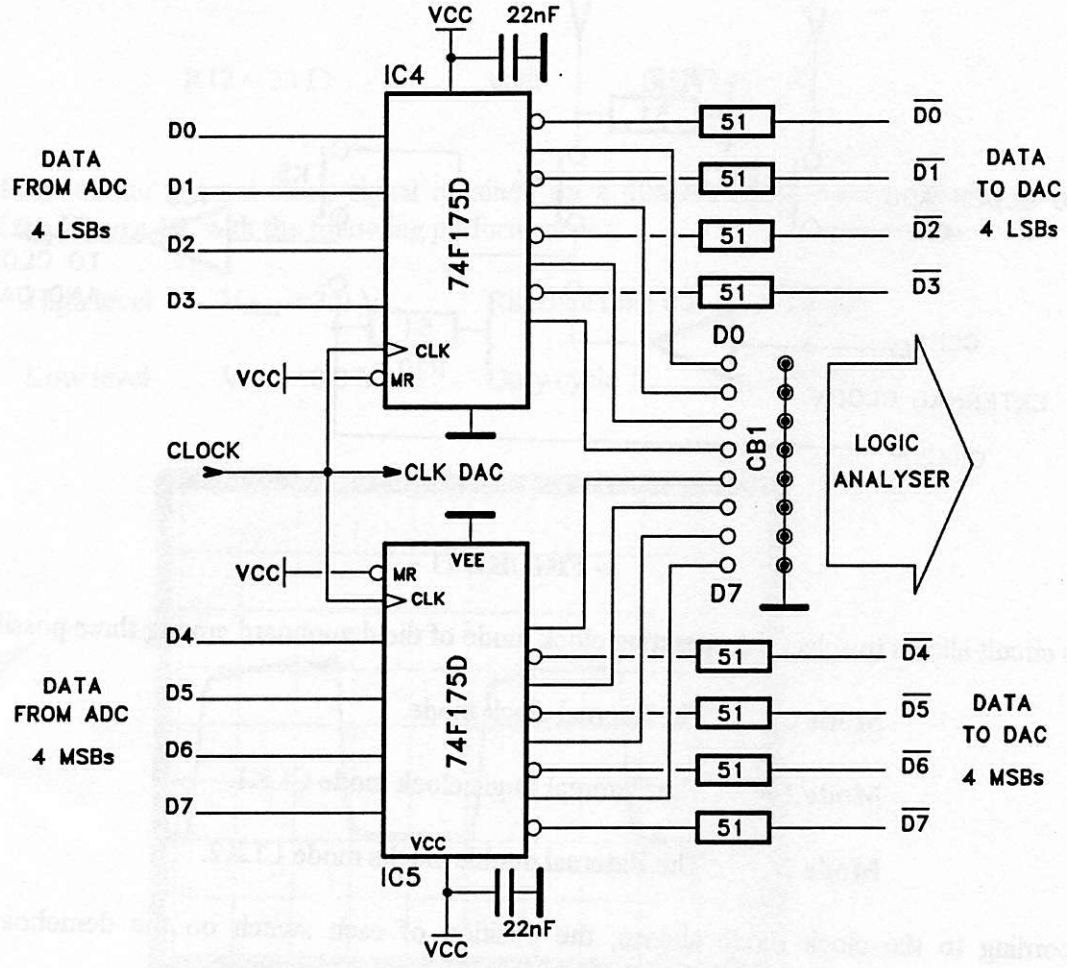
Mode 2 : The External double clocks mode CLK2.

According to the clock mode chosen, the position of each switch on the demoboard is the following :



5.5 TTL INTERFACE CIRCUIT

This circuit, of which the electrical diagram is shown on the **Figure 12**, allows to recover the ADC data output synchronized on the clock sampling edge rising.



- FIGURE 12 -

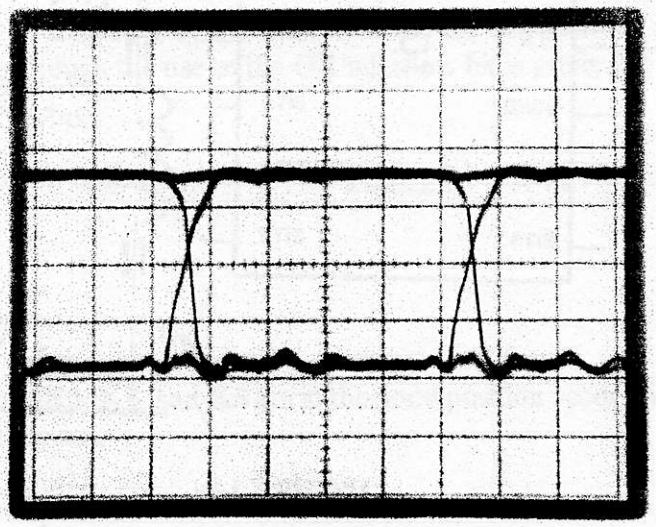
The interface circuit uses two SMD ICs D Flip-Flop type **74F175D** of the Fast TTL Logic Family, [5].

The recovered data are directly addressed to the special probe connector CB1, while the complementary data outputs are addressed to digital inputs Bit 0 to 7 of the DAC, through the damping resistors R21 to R28 and the microstrip lines of characteristic impedance $Z_C = 75\Omega$.

Taking into account the DC output impedance value about $R_O = 25\Omega$, the damping resistor value was fixed at 51Ω in order to satisfy the relation :

$$Z_c = R_{DAMP} + R_0$$

The **Figures 13** shows the recovered eye diagram D0 obtained on the output of the Fast D Flip-Flop, with a internal clock sampling of 40 MS/s.

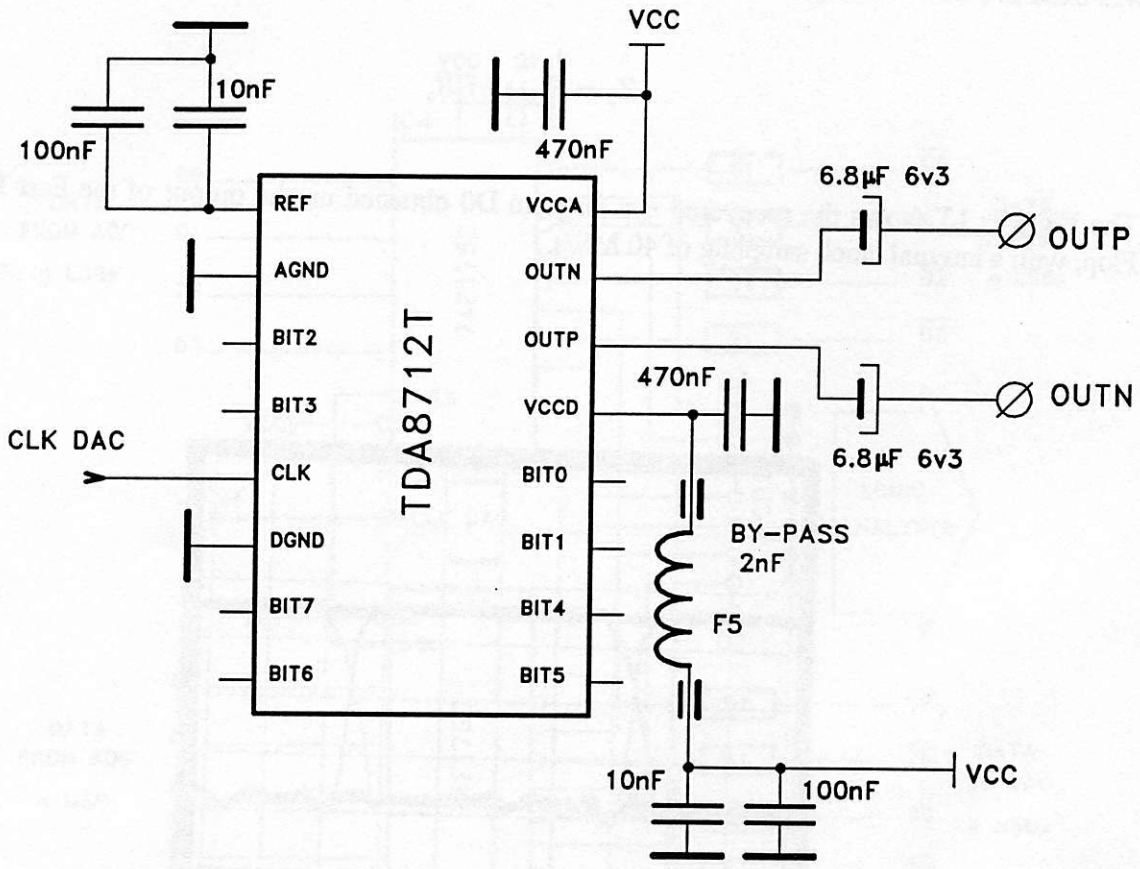


↑ 1 V/div → 5 ns/div

- FIGURE 13 -

5.6 DIGITAL TO ANALOG CONVERTER

In order to reconstruct the analog signal from the Fast complementary data output, the Digital to Analog Converter type TDA8712T (see data sheets in annex) was used with the application diagram shown on the **Figure 14**.



- FIGURE 14 -

A single supply voltage VCC of + 5 Volts is connected to the analog VCCA and digital VCCD pins of the DAC. However, to improve the digital rejection on the VCC, a SMD pi type filter was put close to pin VCCD of the device.

The AC coupling allows to obtain the restored analog signal on the OUTP/N 75Ω BNC connectors.

6. MODES OF OPERATION

An external power unit of 12V/0.5A is necessary to supply the Demoboard. However, the board is able to work between 10 V and 15 V.

Moreover, all DC voltage adjustments were set and locked in Laboratory before delivery to be conform to the provided product specifications. That is to say :

$$V_{RT} = 3.60\ V$$

$$V_{RB} = 1.30\ V$$

$$V_{OFF} = 2.40\ V$$

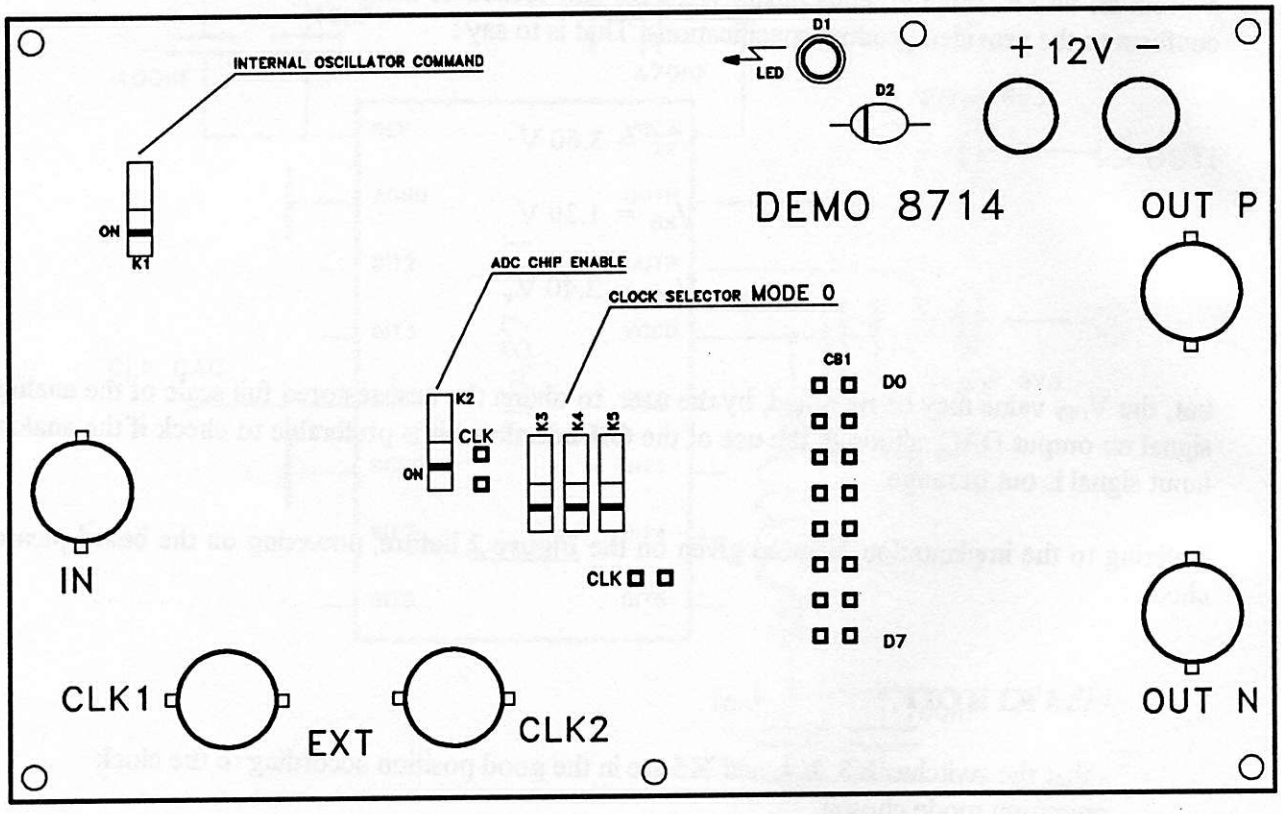
but, the V_{OFF} value may be modified, by the user, to obtain the best restored full scale of the analog signal on output DAC, although the use of the **O/Underflow** bit is preferable to check if the analog input signal is out of range.

Refering to the implantation diagram given on the **Figure 2** before, powering on the board please check :

- that **K1** is **OFF**,
- that the switches **K3**, **K4**, and **K5** are in the good position according to the clock operation mode chosen,
- that the ADC chip enable switch **K2** is **ON**.

6.1 MODE O INTERNAL CLOCK OPERATION

In this mode, the different positions of the switches are given on the **Figure 15**. To switch on the internal clock oscillator, use switch **K1** after the board is powered on.



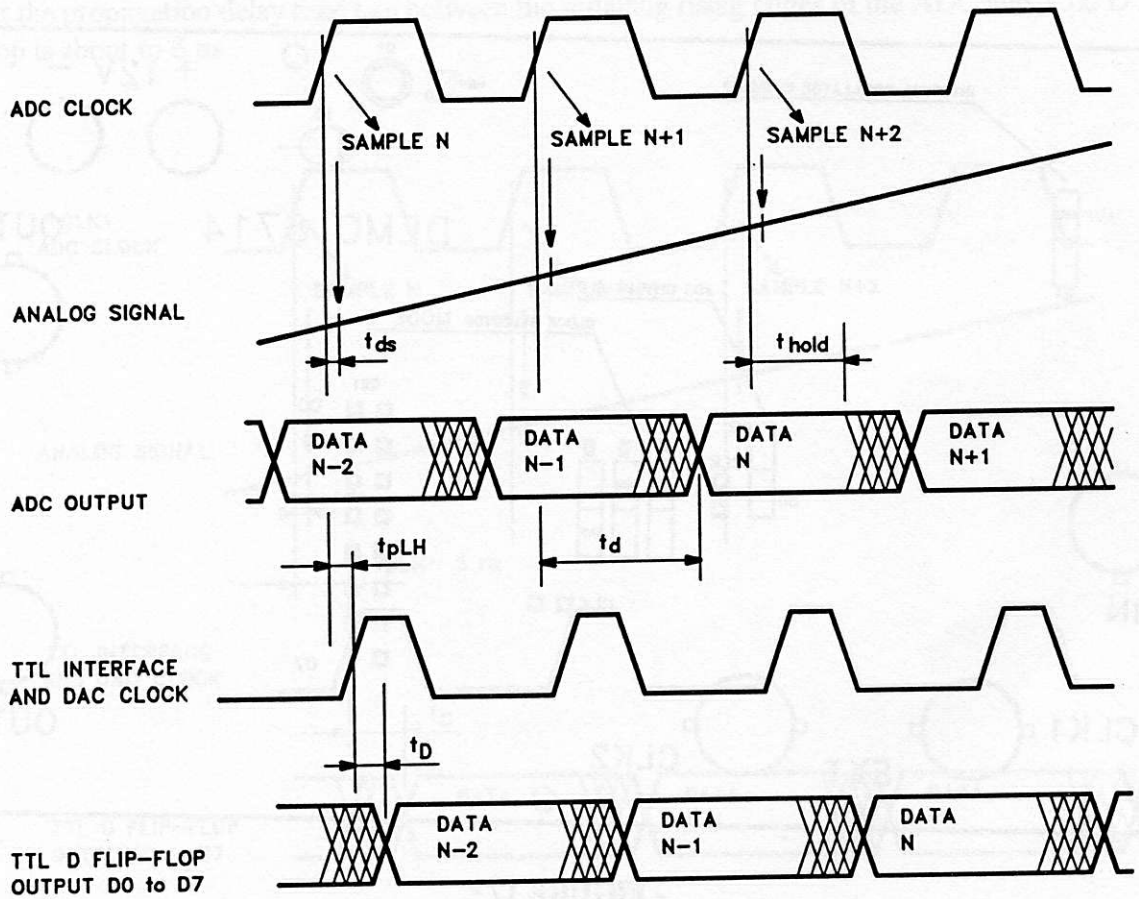
- FIGURE 15 -

Board configuration in order to use the internal clock

The relevant timing of this operating mode is given on the diagram of the **Figure 16**. The particular typical values of the delay times are the following :

- ADC sampling rising edge to D Flip Flop sampling rising edge : t_{pLH} = 3 ns
- D Flip Flop sampling rising edge to data output : t_D = 5 ns

For the timing diagram of the TDA8714 please refer to the product specifications of the device (see annex).



- FIGURE 16 -

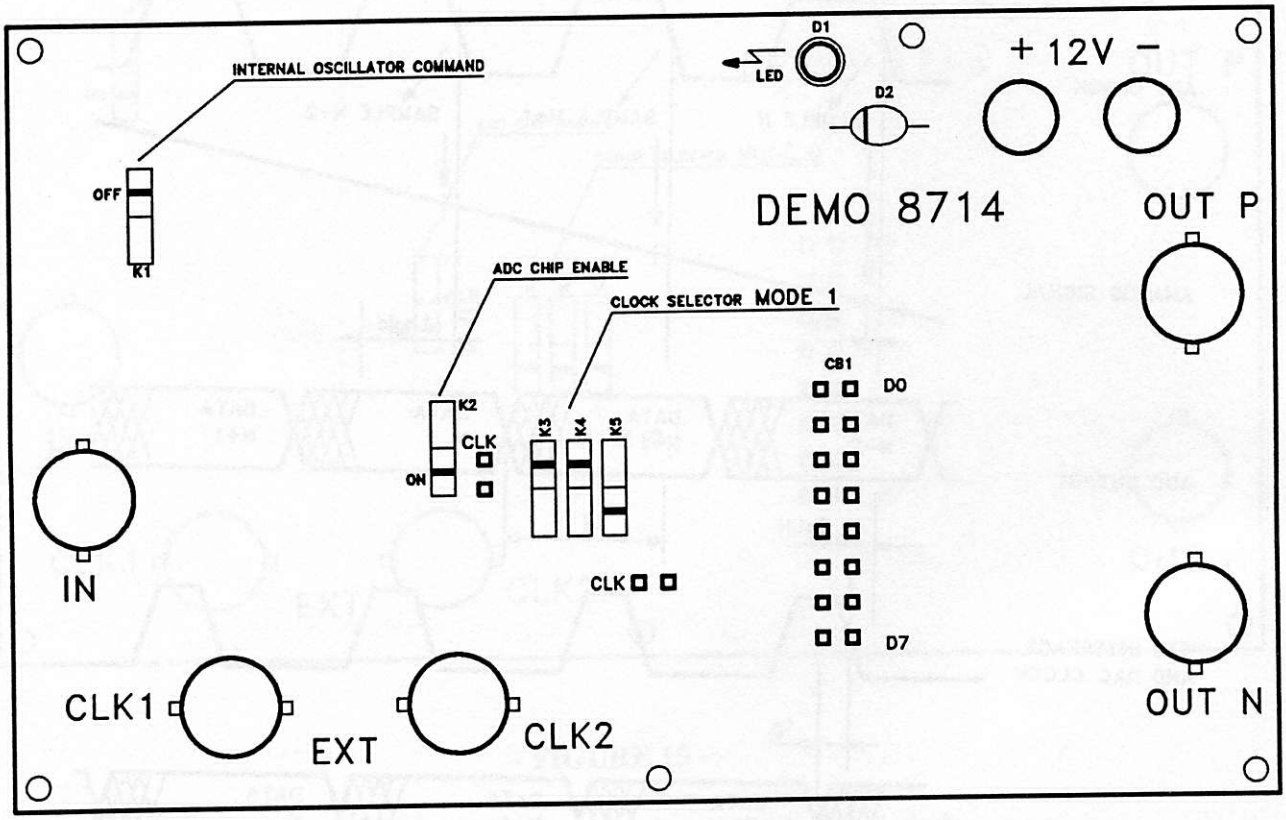
Timing diagram with internal clock mode

6.2 MODE 1 EXTERNAL SINGLE CLOCK OPERATION

In this mode, the position of the different switches are given on the Figure 17.

- The internal clock oscillator is set **OFF** with switch **K1**.

- The 50Ω BNC external clock input **CLK1** is used to connect an external 50Ω clock generator.



- FIGURE 17 -

Board configuration in order to use the external single clock

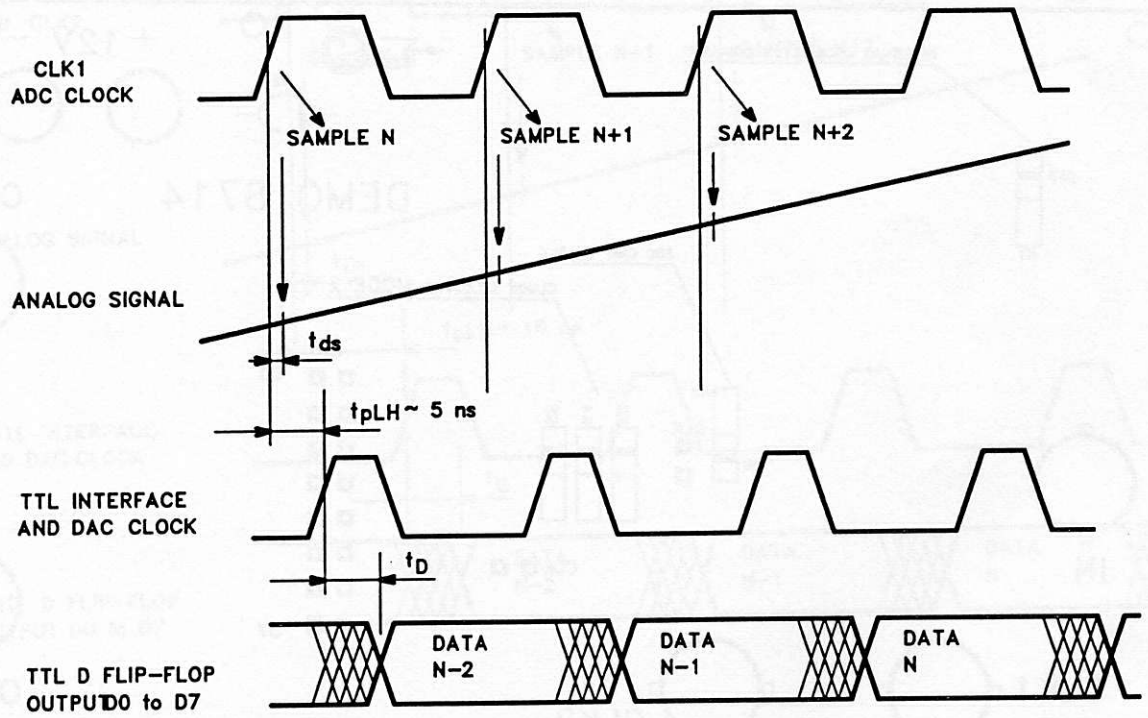
The required clock levels are the following :

$$V_{CLKH} \text{ min} = 2.0 \text{ V}$$

$$V_{CLKL} \text{ max} = 0.8 \text{ V}.$$

In order to restore a good timing, the clocks of the TTL interface circuit and DAC are derived from the clock of the ADC through two TTL inverters type 74F04.

Thereby, the timing diagram given on the **Figure 18** is almost the same as the timing of the mode 0, but the propagation delay time t_{pLH} between the sampling rising edges of the ADC and TTL D Flip-Flop is about to **5 ns** .



- FIGURE 18 -

Timing diagram with external single clock

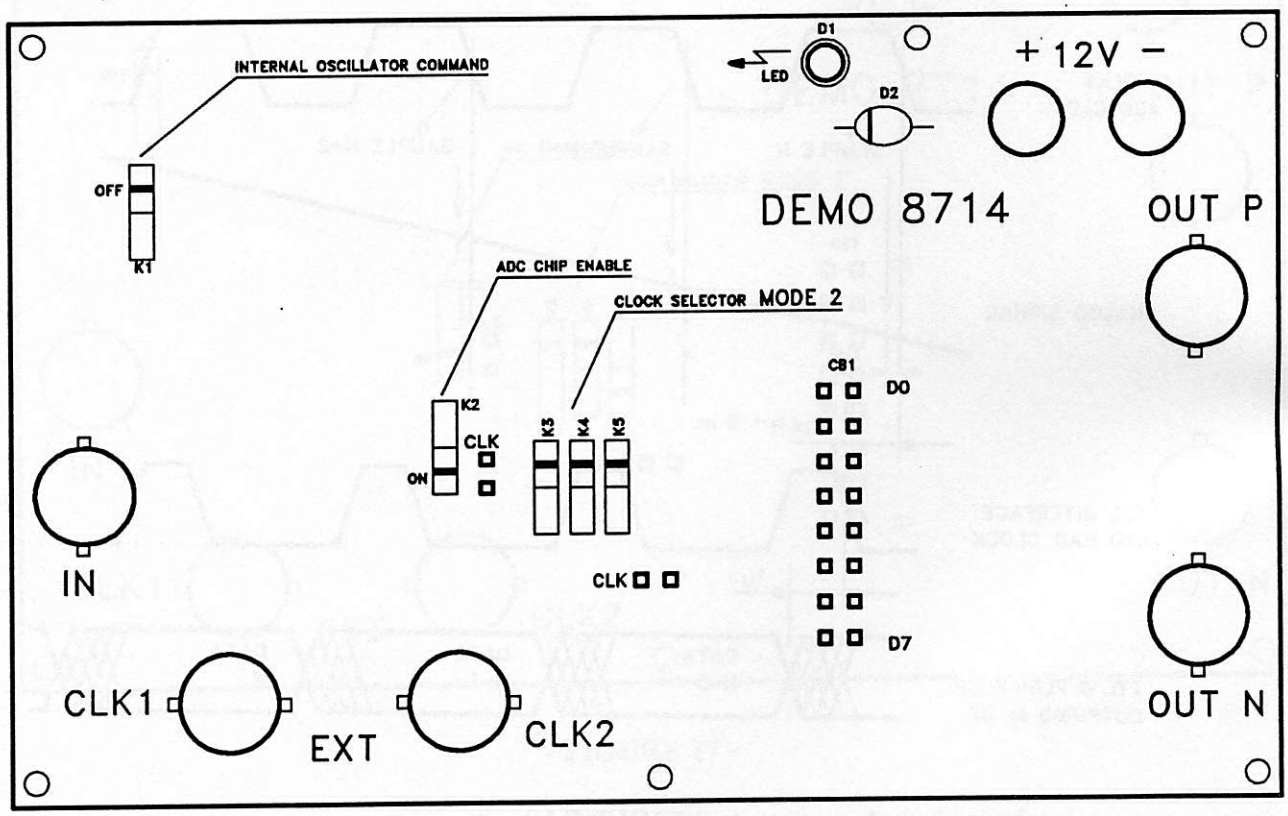
6.3 MODE 2 EXTERNAL TWO CLOCK OPERATION

This operating mode allows to use two clocks at the same frequency for the ADC and the DAC whose clock is derived from the TTL interface circuit clock. The **Figure 19** shows the board configuration in order to use this mode.

- The internal clock oscillator is set **OFF** with the switch **K1**.

- The 50Ω BNC external clock input **CLK1** is used for the ADC clock. But, now the 50Ω BNC external clock input **CLK2** is used for the TTL D Flip-Flop interface circuit.

So, the user will be able to adjust the phase of the TTL intreface circuit and DAC clock, if necessary.



- FIGURE 19 -

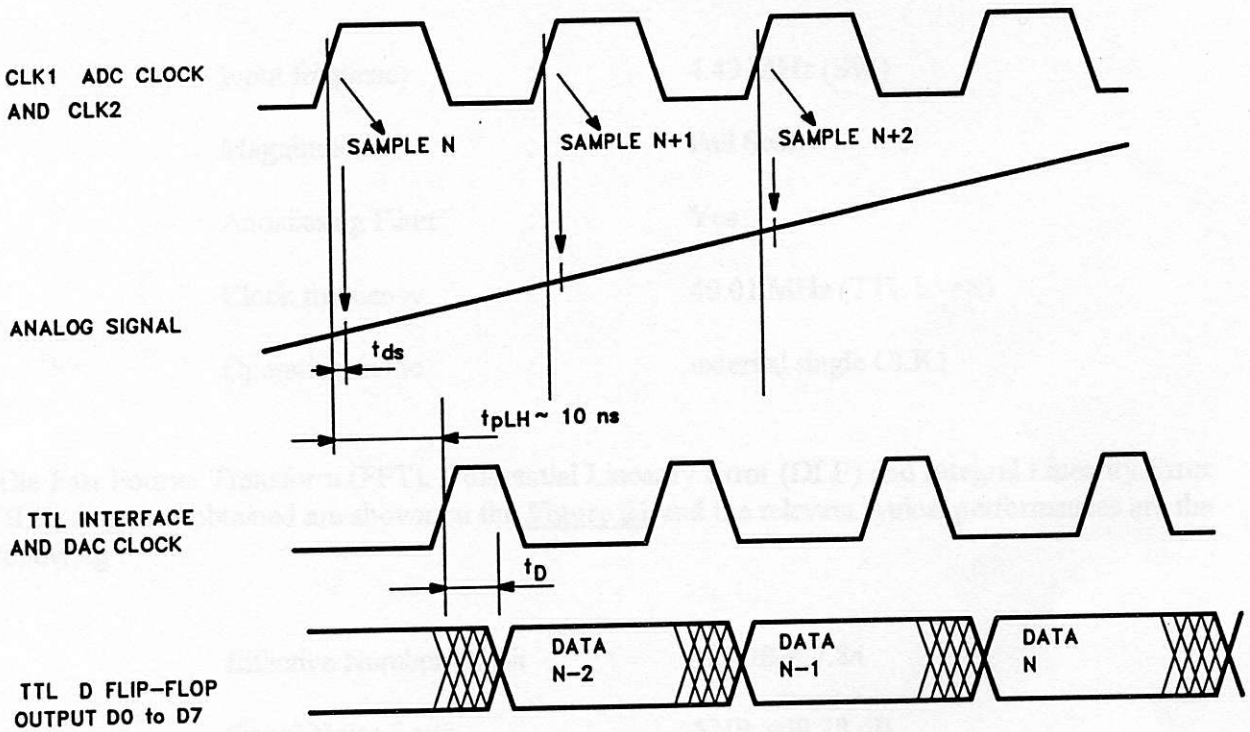
Board configuration in order to use two external clocks

The required clock levels on the inputs CLK1 and CLK2 are the following :

$$V_{CLKH} \text{ min} = 2.0 \text{ V}$$

$$V_{CLKL} \text{ max} = 0.8 \text{ V}.$$

The timing diagram is given on the **Figure 20**. With the two clocks CLK1 and CLK2 in phase, the delay time between the ADC and the D Flip-Flop sampling rising edge is about to **10 ns**.



- FIGURE 20 -

Timing diagram with two external clocks

7. PERFORMANCES

An evaluation of the performances of the TDA8714T Analog to Digital Converter was made with the demoboard environment. Two versions of the demoboard (40 and 75MS/s) were evaluated on the Caen's dynamic bench.

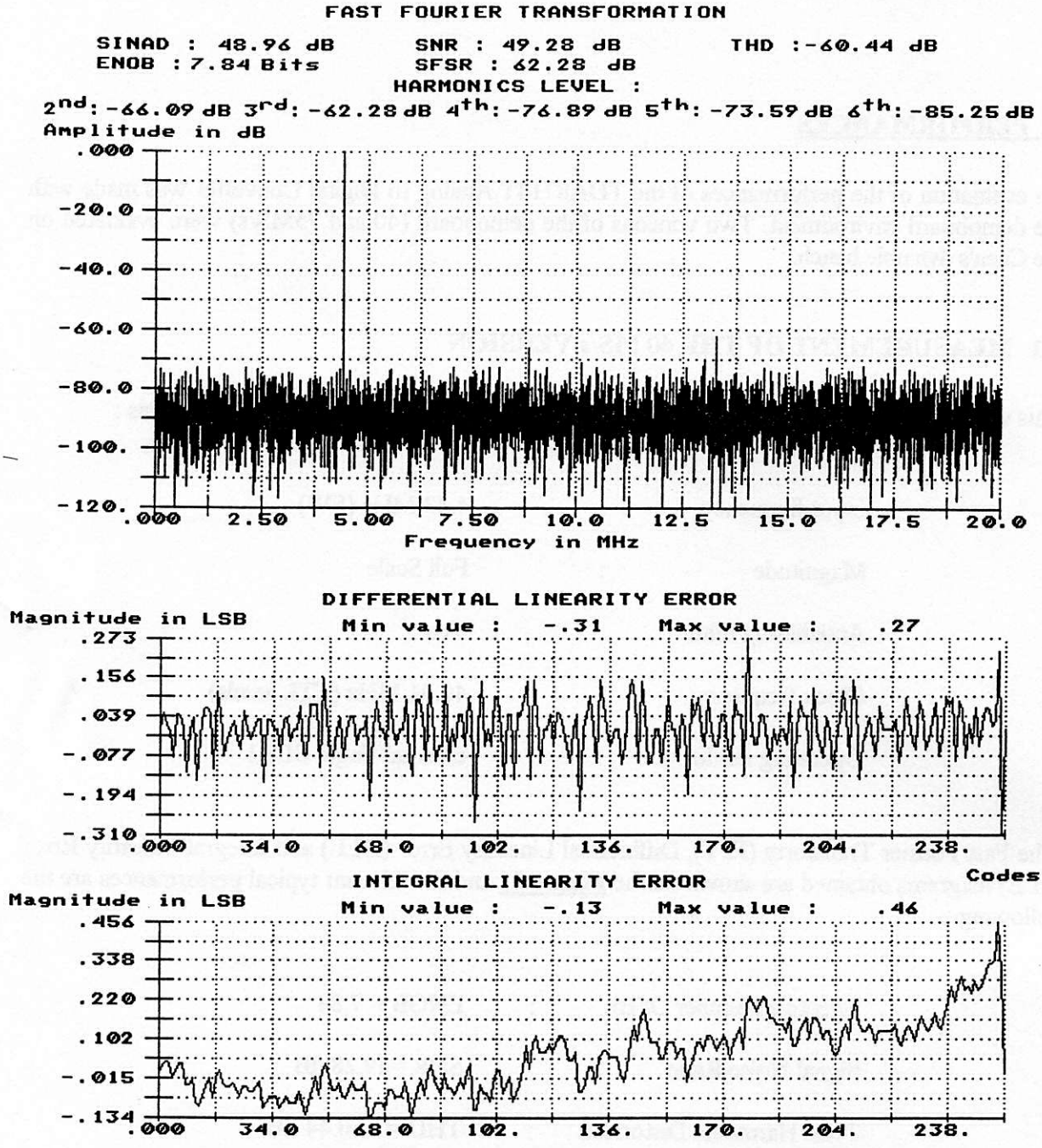
7.1 MEASUREMENT OF THE 40 MS/s VERSION

This version of the demoboard, was evaluated with the following measurement conditions :

Input frequency	:	4.43 MHz (SW)
Magnitude	:	Full Scale
Antialiasing Filter	:	Yes
Clock frequency	:	40.01 MHz (TTL levels)
Operating mode	:	external single CLK1

The Fast Fourier Transform (FFT), Differential Linearity Error (DLE) and Integral Linearity Error (ILE) diagrams obtained are shown on the **Figure 21** and the relevant typical performances are the following :

Effective Number Of Bit	:	ENOB = 7.84
Signal Noise Ratio	:	SNR =49.28 dB
Total Harmonic Distorsion	:	THD = - 60.44 dB
Differential Linearity Error	:	$\|DLE\| \leq 0.31$
Integral Linearity Error	:	$\|ILE\| < 0.46$



- FIGURE 21 -

40 MS/s sampling frequency - 4.43 MHz analog frequency
FFT - DLE - and ILE diagrams

7.2 MEASUREMENT OF THE 75 MS/s VERSION

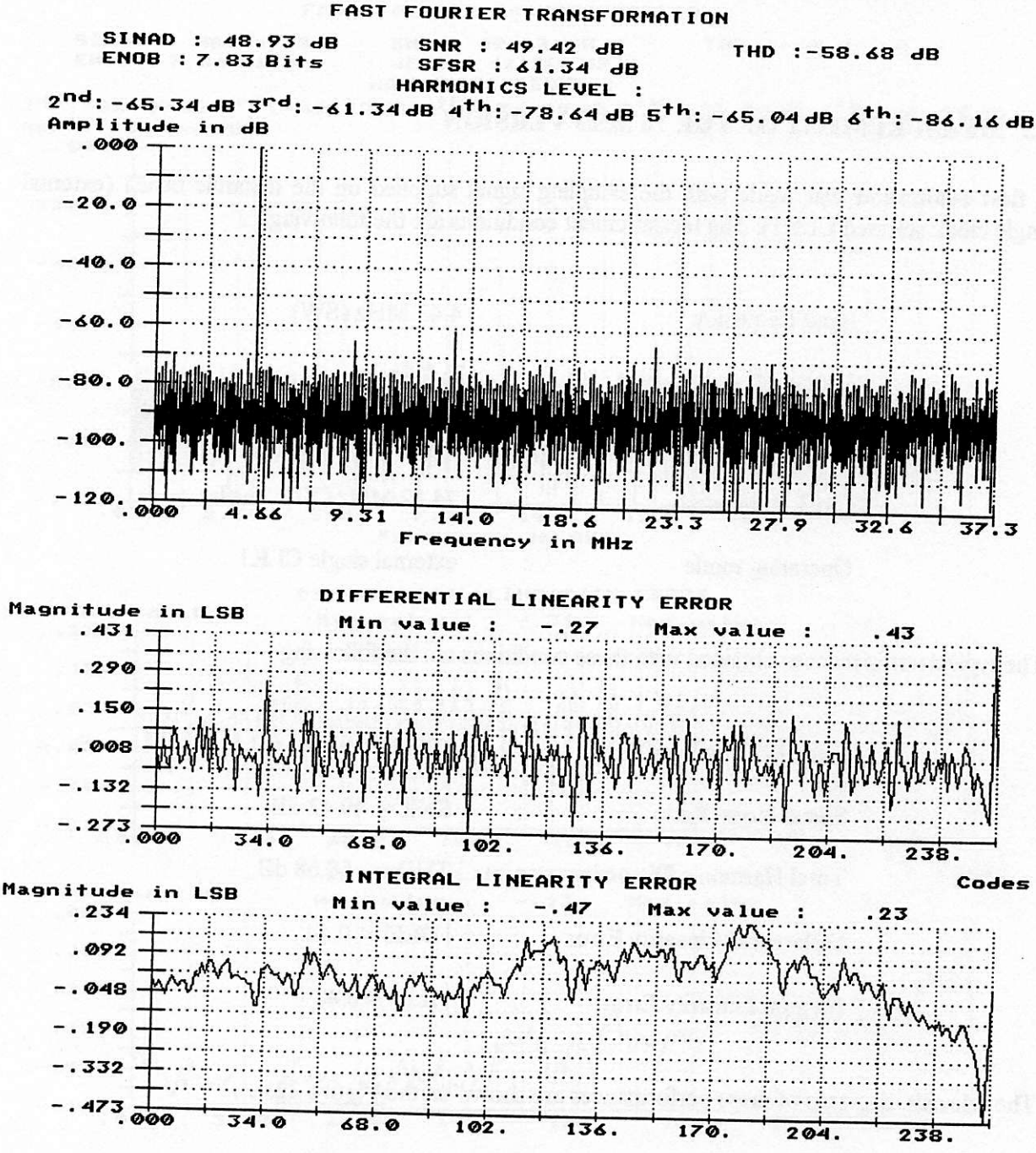
A **first evaluation** was made with the sampling signal supplied on the dynamic bench (external single clock selected CLK1). The measurement conditions are the following :

Input frequency	:	4.43 MHz (SW)
Magnitude	:	Full Scale
Antialiasing Filter	:	Yes
Clock frequency	:	74.52 MHz (TTL levels)
Operating mode	:	external single CLK1

The typical performances obtained with these conditions are the following :

Effective Number Of Bit	:	ENOB = 7.83
Signal Noise Ratio	:	SNR = 49.42 dB
Total Harmonic Distorsion	:	THD = - 58.68 dB
Differential Linearity Error	:	$\|DLE\| < 0.44$
Integral Linearity Error	:	$\|ILE\| < 0.48$

The relevant diagrams of these performances are shown on the **Figure 22**.



- FIGURE 22 -

74.52 MS/s sampling frequency - 4.43 MHz analog frequency
FFT - DLE and ILE diagrams

The **second evaluation** was made with the sampling signal supplied on the demoboard (internal clock selected). The measurement conditions are :

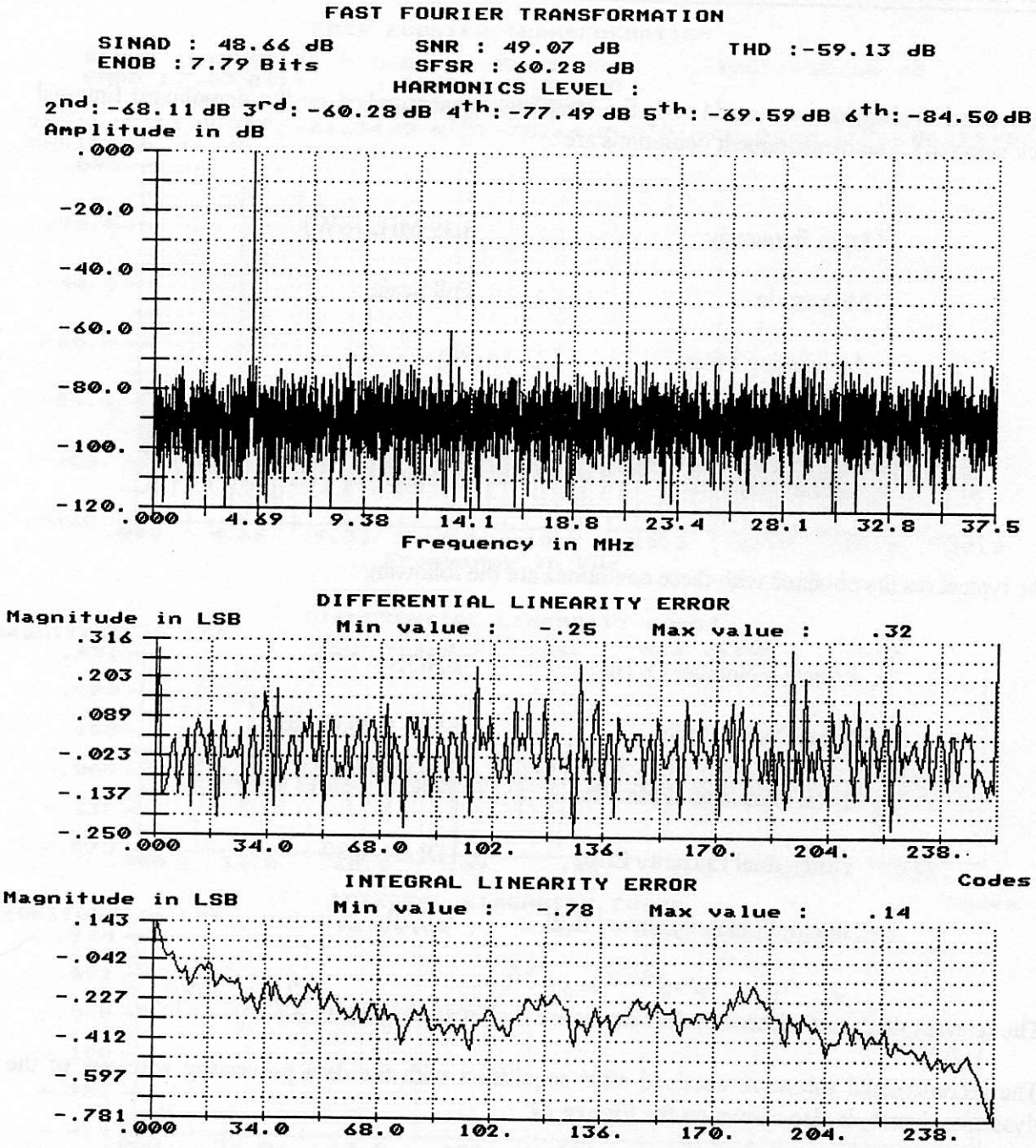
Input frequency	:	4.39 MHz (SW)
Magnitude	:	Full Scale
Antialiasing Filter	:	No
Clock frequency	:	75.00 MHz (TTL levels)
Operating mode	:	Internal

The typical results obtained with these conditions are the following :

Effective Number Of Bit	:	ENOB = 7.79
Signal Noise Ratio	:	SNR = 49.07 dB
Total Harmonic Distorsion	:	THD = - 59.13 dB
Differential Linearity Error	:	$\|DLE\| \leq 0.32$
Integral Linearity Error $\|ILE\|$	:	< 0.79

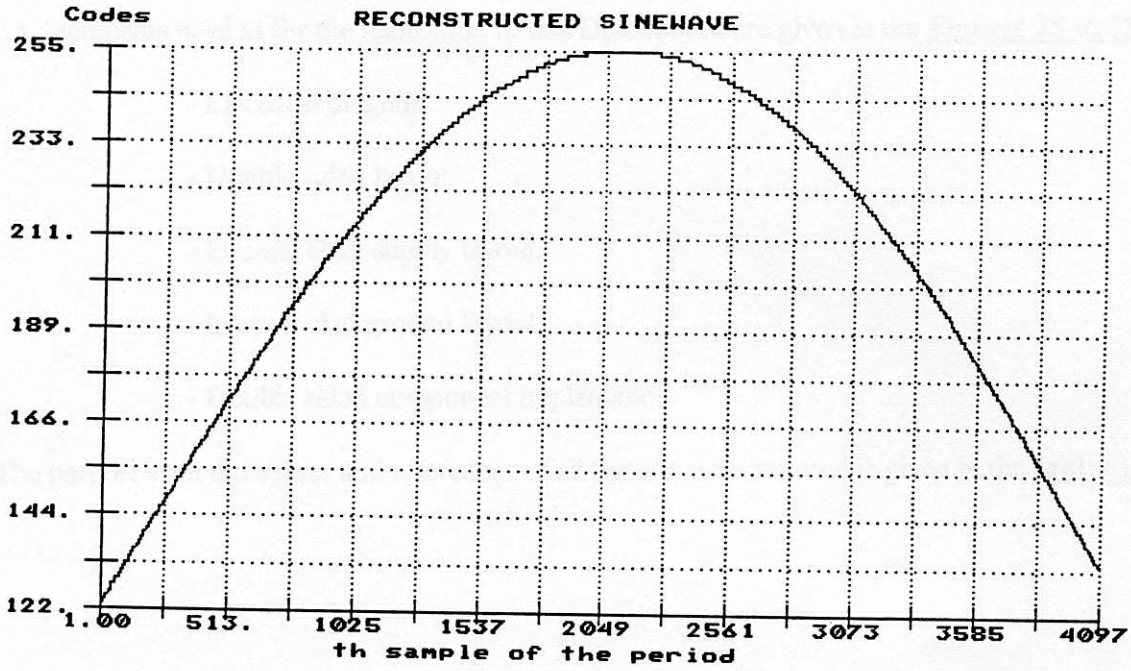
The relevant diagrams of these performances are shown on the **Figure 23**.

The reconstructed sinewave obtained after acquisition with the data processing software of the dynamical bench, is also shown on the **Figure 24**.



- FIGURE 23 -

75 MS/s sampling frequency - 4.39 MHz analog frequency
FFT - DLE and ILE diagrams



- FIGURE 24 -

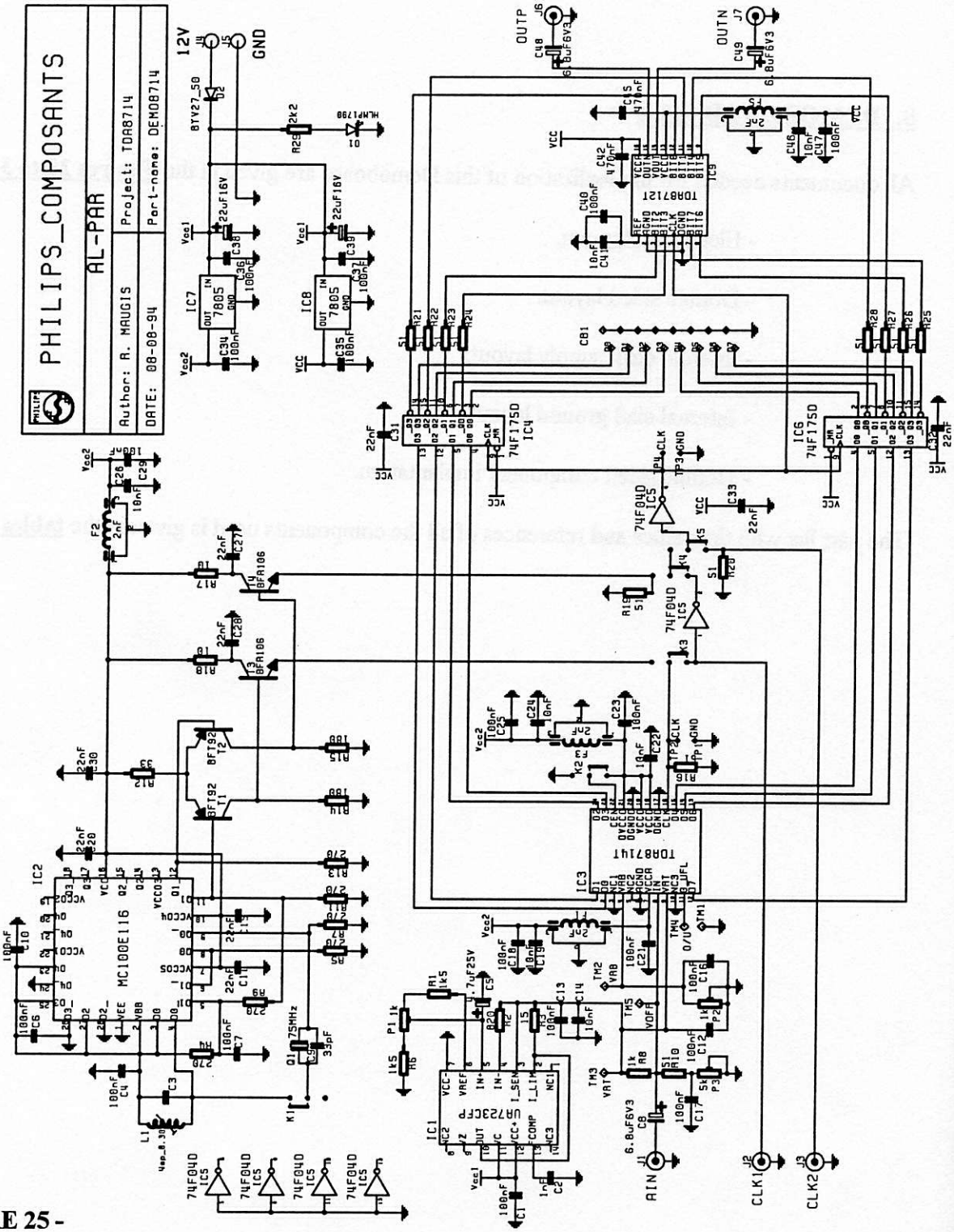
75 MS/s sampling frequency - 4.39 MHz analog frequency
Reconstructed sinewave

8. DEMOBOARD FILE

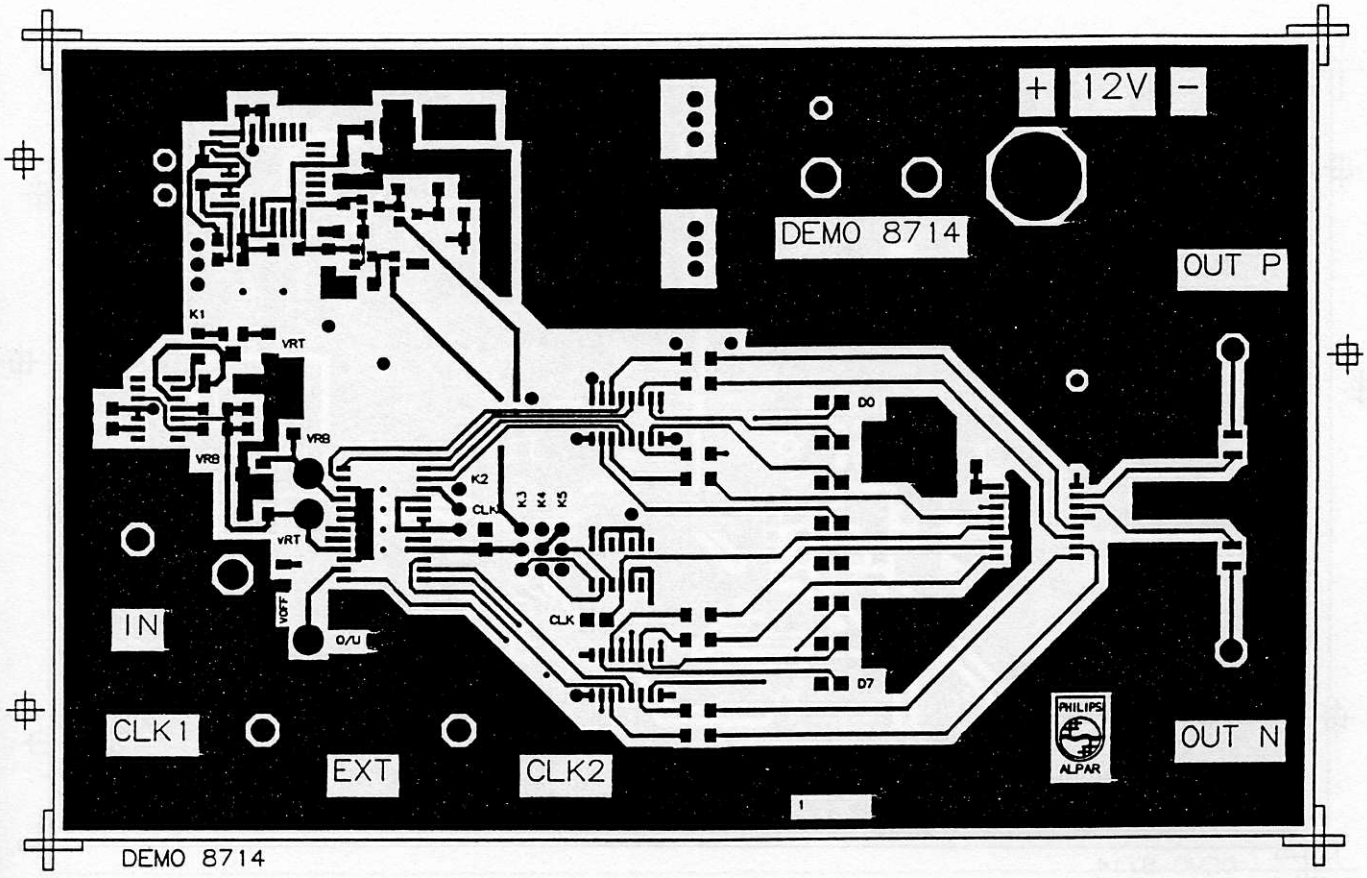
All documents needed for the realization of this Demoboard are given in the **Figures 25 to 31**.

- Electrical diagram.
- Double sided layout.
- Internal clad supply layout.
- Internal clad ground layout.
- Double sided component implantation.

The part list with the values and references of all the components used is given in the **tables 1 to 4**.

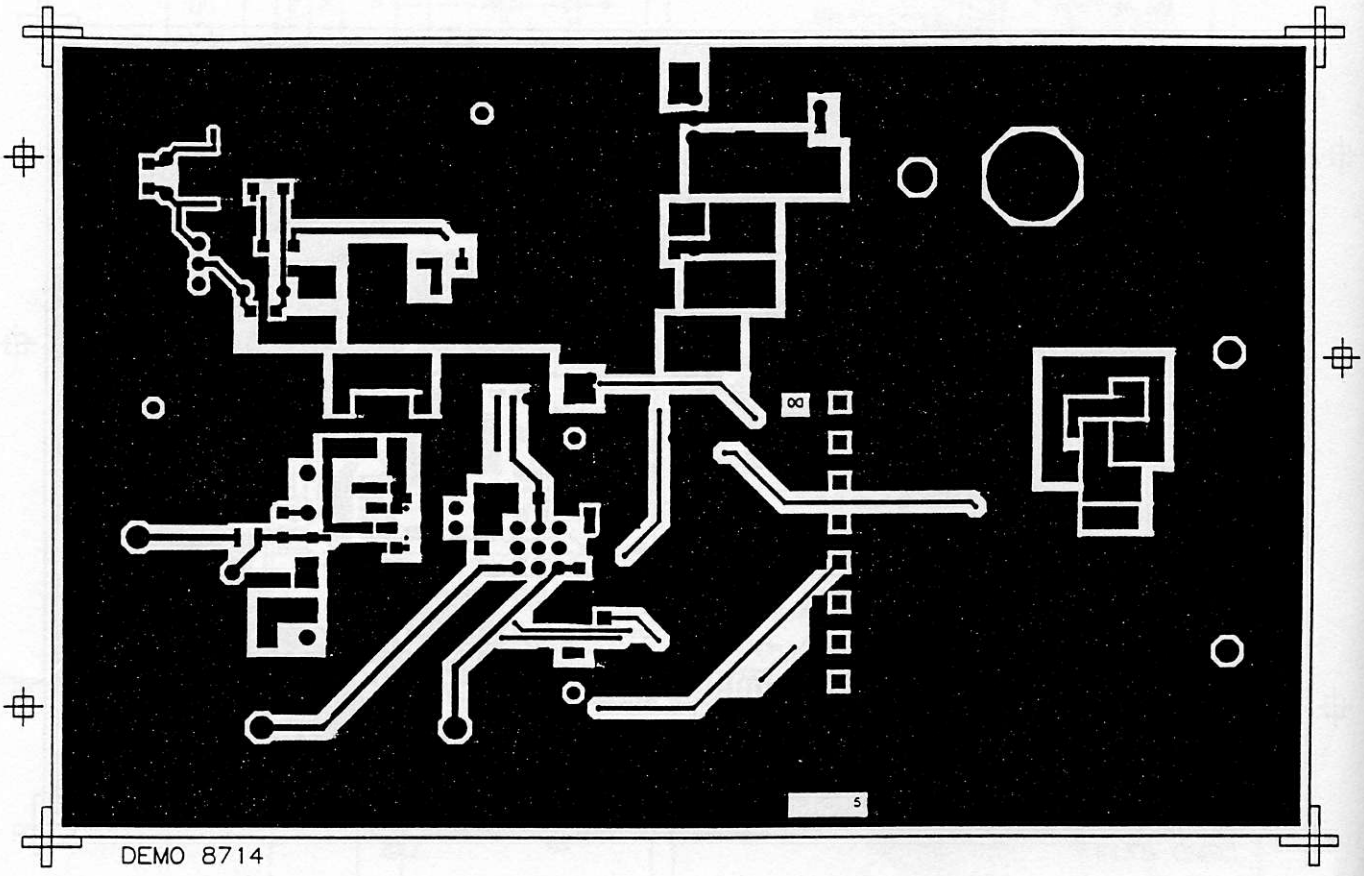

PHILIPS_COMPOSANTS
AL-PAR
Author: R. MAUGIS
Project: TDA8714
Part-name: DEMO8714
DATE: 08-08-94
12V
GND
OUTP
OUTN
AIN
CLK1
CLK2
TDA8712T
TDA8714T
74F175D
74F04D
MC100E116
GA723CFP
BFR106
BF192
7805
BTY27_50
HLMP1790

- FIGURE 25 -



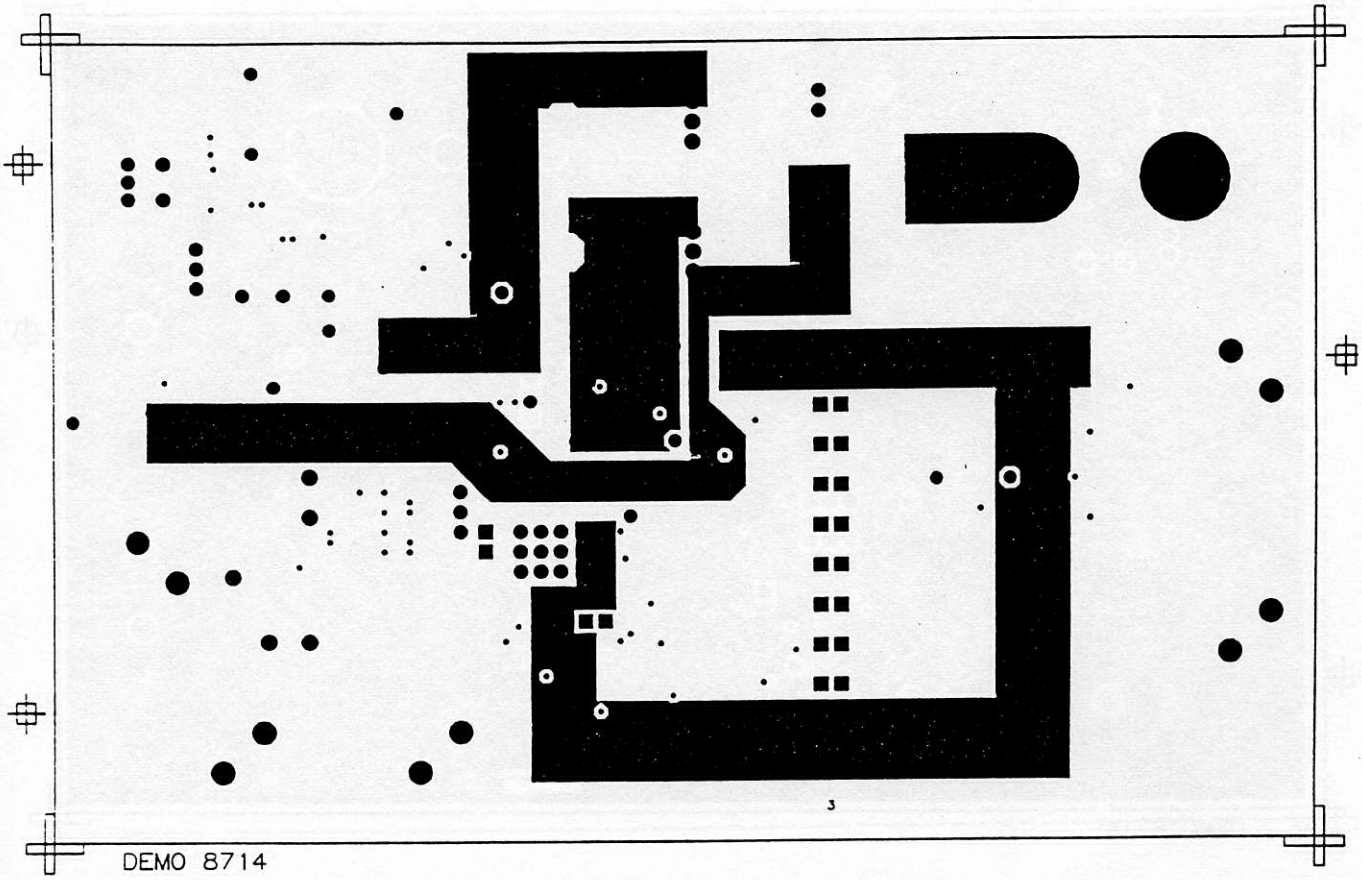
- FIGURE 26 -

Overside layout (signal layer 1)



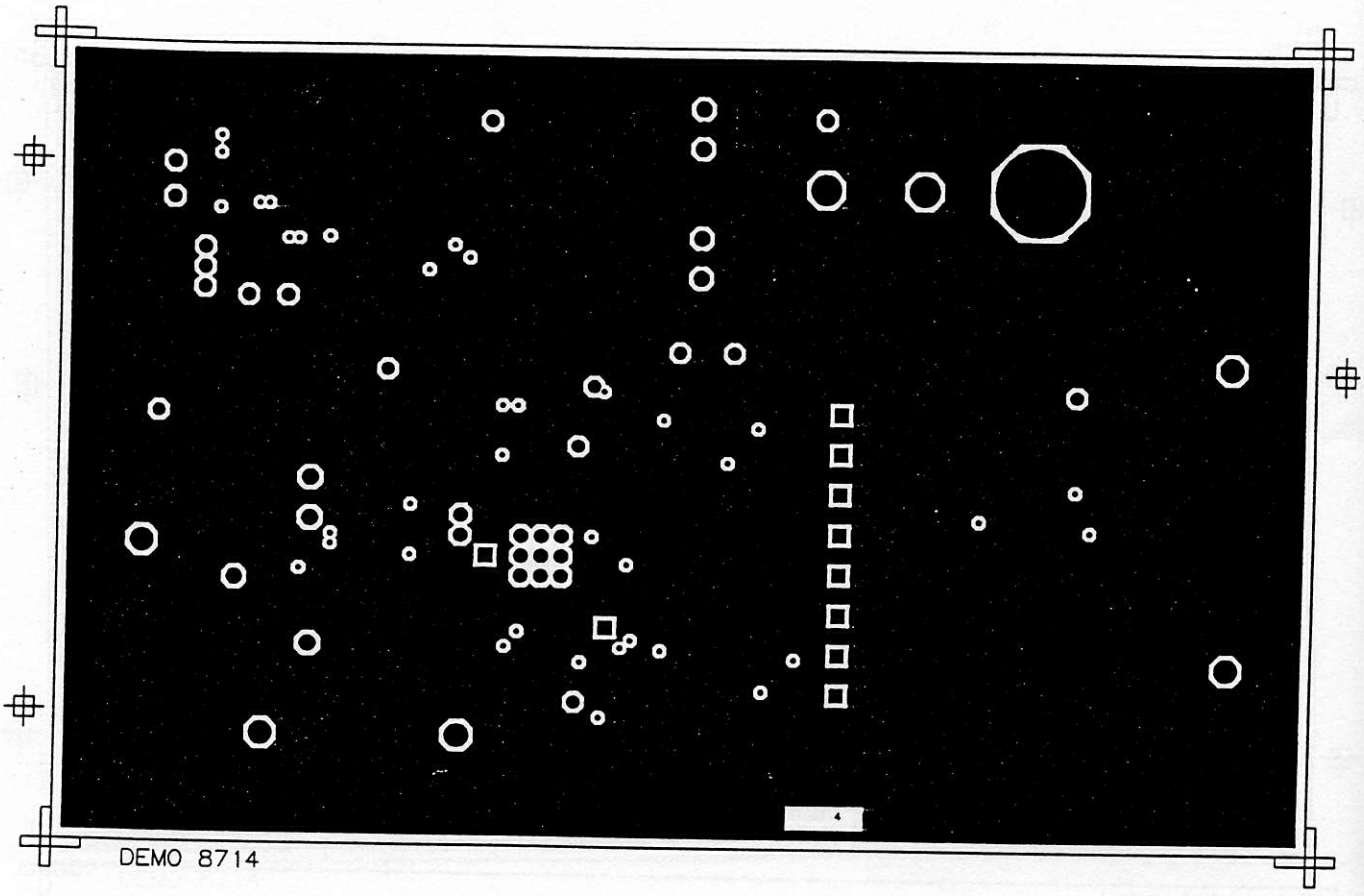
- FIGURE 27 -

Underside layout (signal layer 5)



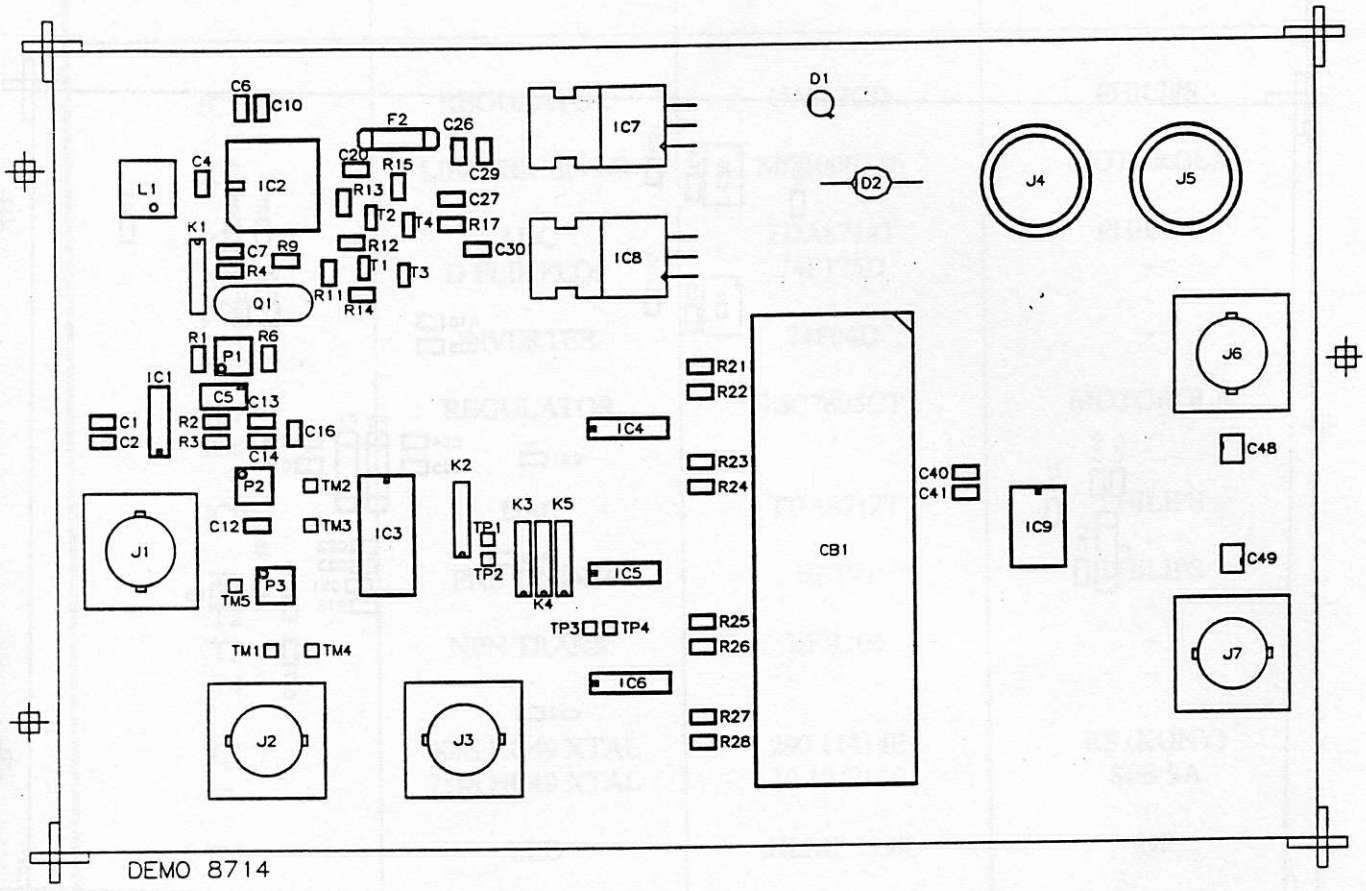
- FIGURE 28 -

Internal layout (supply layer 3)



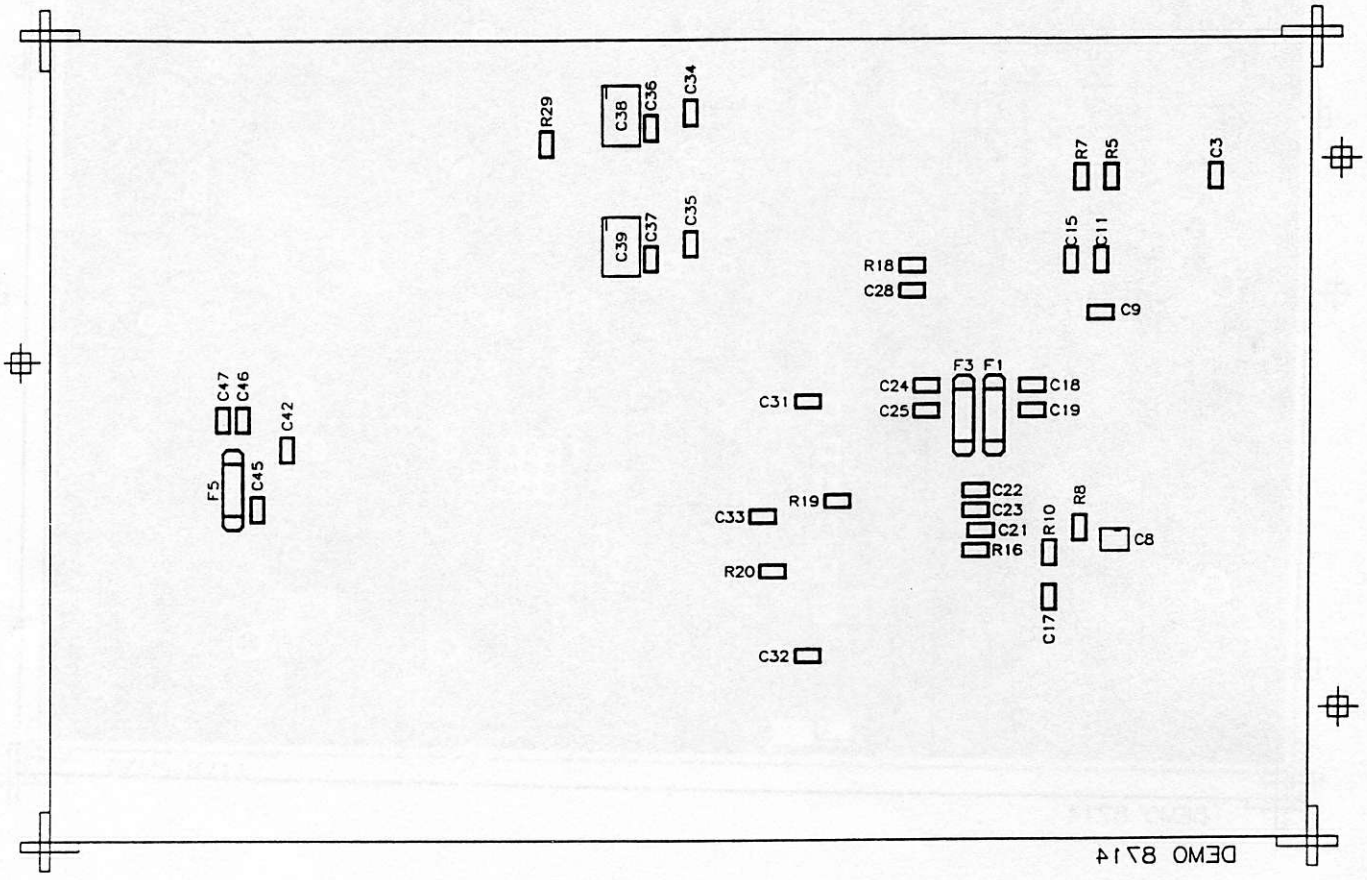
- FIGURE 29 -

Internal layout (ground layers 2 and 4)



- FIGURE 30 -

Overside components implantation



- FIGURE 31 -

Underside components implantation

REFERENCES	VALUES	CODE NUMBER	MANUFACTURER
IC1	REGULATOR	UA723CD	PHILIPS
IC2	LINE RECEIVER	MC100E116	MOTOROLA
IC3	ADC	TDA8714T	PHILIPS
IC4	D FLIP FLOP	74F175D	-
IC6	-	-	-
IC5	INVERTER	74F04D	-
IC7	REGULATOR	MC7805CT	MOTOROLA
IC8	-	-	-
IC9	DAC	TDA8712T	PHILIPS
T1	PNP TRANS.	BFT92	PHILIPS
T2	-	-	-
T3	NPN TRANS.	BFR106	-
T4	-	-	-
Q1	40M HC49 XTAL	290 11414E	RS (KONY)
-	75M HC49 XTAL	10 10 20 30	SPS SA
D1	LED	HLMP 1790	HP
D2	DIODE	BYV27 50	PHILIPS
F1	PI FILTER 2nF	SK 7076 001 S	TUSONIX
F2	-	-	-
F3	-	-	-
F4	-	-	-
L1	SELF 4SP/0.3	7_1S	TOKO
CB1	TEST PROBE	8X TEST POINT	COMATEL

- TABLE 1 -

REFERENCES	VALUES	CODE NUMBER	MANUFACTURER
R1	SMD 1.5kΩ	RC02GP 1K5	PHILIPS
R6	-	-	-
R2	SMD 820 Ω	RC02GP 820	-
R3	SMD 15 Ω	RC02GP 15	-
R8	SMD 1 kΩ	RC02GP 1K	-
R4	SMD 270 Ω	RC02GP 270	-
R5	-	-	-
R7	-	-	-
R9	-	-	-
R11	-	-	-
R13	-	-	-
R14	-		-
R15	SMD 180 Ω	RC02GP 180	-
R17	-	-	-
R18	SMD 10 Ω	RC02GP 10	-
R12	-	-	-
R10	SMD 33 Ω	RC02GP 33	-
R16	SMD 51 Ω	RC02GP 51	-
R19	-	-	-
R20	-	-	-
R21	-	-	-
R22	-	-	-
R23	-	-	-
R24	-	-	-
R25	-	-	-
R26	-	-	-
R27	-	-	-
R28	-	-	-
R29	SMD 2.2kΩ	RC02GP 2K2	-
P1	POTENTIOMETER	3224 W 1K	BOURNS
P2	-	-	-
P3	-	3224 W 5K	-
K1 to K5	SWITCH 1C2P	09 03201 02	SECME

- TABLE 2 -

REFERENCES	VALUES	CODE NUMBER	MANUFACTURER
C1	SMD 100 nF	1206 2R104K9	PHILIPS
C4	-	-	-
C6	-	-	-
C7	-	-	-
C10	-	-	-
C12	-	-	-
C13	-	-	-
C16	-	-	-
C17	-	-	-
C18	-	-	-
C21	-	-	-
C23	-	-	-
C25	-	-	-
C29	-	-	-
C34	-	-	-
C35	-	-	-
C36	-	-	-
C37	-	-	-
C40	-	-	-
C47	-	-	-
C14	SMD 10 nF	1206 2R103K9	PHILIPS
C19	-	-	-
C22	-	-	-
C24	-	-	-
C26	-	-	-
C41	-	-	-
C46	-	-	-
C11	SMD 22nF	1206 2R223K9	PHILIPS
C15	-	-	-
C20	-	-	-
C27	-	-	-
C28	-	-	-
C30 to C33	-	-	-

- TABLE 3 -

REFERENCES	VALUES	CODE NUMBER	MANUFACTURER
C2	SMD 1 nF	1206 2R102K9	PHILIPS
C3	SMD 56 pF	1206 2R560K9	-
C9	SMD 33 pF	1206 2R330K9	-
C42	SMD 470 nF	1206 2R474K9	PHILIPS
C45	-	-	-
C38	SMD 22µF 16V	293D226X9016D	SPRAGE
C39	-	-	-
C8	SMD 6.8µF 6V3	293D685X96R3B	SPRAGE
C48	-	-	-
C49	-	-	-
C5	SMD 4.7µF 25V	293D475X9025C	SPRAGE
J1	BNC 50Ω	R 141 426 161	RADIALL
J2	-	-	-
J3	-	-	-
J6	-	-	-
J7	-	-	-
J4	BANANA PLUG	R 941 921	RADIALL
J5	-	R 941 920	-
TP1 to TP4	TEST POINT	3850358102400	COMATEL
TM1 to TM5	BOLT HOLD	3110415000530	COMATEL
	-		

- TABLE 4 -

ANNEX

TDA8714	**DATA SHEET**	**JUNE 1994**
TDA8712	**DATA SHEET**	**JUNE 1994**